C.V.RAMAN POLYTECHNIC, BHUBANESWAR

LESSON PLAN
Session (2026-2027)

Discipline: ELECTRICAL ENGINEERING	**Semester:**5th Semester, Winter/2026	**Name of the Faculty:** SUCHISMITA SATPATHY ASST.PROF **Email ID: suchismita@cvrp.edu.in**
Subject Name with code: DIGITAL ELECTRONICS AND MICROPROCESSOR (EEPC301)	**No.of Days/week:**03 **Total No. of Class (Required):** 45	**Start Date: 01.07.2026** **End Date: 5.11.2026**

Week	Class Day	Brief description of the Topic/Chapter to be taught
1st	1st	**Digital Fundamentals Number Systems :** Decimal, Binary, Octal, Hexadecimal.
	2nd	1's and 2's complements.
	3rd	Codes – Binary, BCD, Excess 3, Gray, Alphanumeric codes.
2nd	1st	Boolean theorems, Logic gates and truth tables, Universal gates.
	2nd	Sum of products and product of sums, Min terms and Max terms,
	3rd	Karnaugh map Minimization.
3rd	1st	QuineMc Cluskey method of minimization.
	2nd	**Combinational & Synchronous Sequential Circuits:** Design of Half and Full Adders.
	3rd	Half and Full Subtractors.
4th	1st	Binary Parallel Adder –Multiplexer.
	2nd	Demultiplexers, Decoders, and Priority Encoder.
	3rd	Flip flops – SR, JK, T, D.
	1st	Design of clocked sequential circuits.

5th	2nd	Design of Counters.
	3rd	Shift registers, Universal Shift Register.
6th	1st	Doubt Clearing class and Quiz.
	2nd	**Asynchronous Sequential Circuits And Memory Devices:** Stable and Unstable states, output specifications.
	3rd	Cycles and races, state reduction, race free assignments.
7th	1st	Hazards, Essential Hazards, Pulse mode sequential circuits.
	2nd	Design of Hazard free circuits. Basic memory structure – ROM -PROM – EPROM.
	3rd	EEPROM –EAPROM, RAM – Static and dynamic RAM.
8th	1st	Programmable Logic Devices – Programmable Logic Array (PLA).
	2nd	Programmable Array Logic (PAL).
	3rd	Field Programmable Gate Arrays (FPGA).
9th	1st	Doubt Clearing class and Quiz.
	2nd	**8085 Processor:** Hardware Architecture.
	3rd	Pin diagram – Functional Building Blocks of Processor.
10th	1st	Memory organization – I/O ports and data transfer concepts.
	2nd	Timing Diagram.
	3rd	Interrupts.
11th	1st	Doubt Clearing class and Quiz.
	2nd	**Programming Processor Instruction:** format and addressing.
	3rd	Modes – Assembly language format.
12th	1st	Data transfer, data manipulation & control instructions
	2nd	Data transfer, data manipulation & control instructions
	3rd	Programming: Loop structure with counting.
13th	1st	Programming: Loop structure with counting.
	2nd	Indexing – Look up table.
	3rd	Subroutine instructions.
	1st	Stack.

14th	2nd	8255 architecture and operating modes.
	3rd	8255 architecture and operating modes.
15th	1st	Doubt clearing class and Quiz.
	2nd	Previous year Question Discussion.
	3rd	Previous year Question Discussion.

Signature of the Faculty

Signature of the H.O.D