C. V. RAMAN POLYTECHNIC, BHUBANESWAR

LESSON PLAN
Session (2026-2027)

Discipline: Electronics & Telecommunication Engineering	**Semester:** 3rd Semester, Winter/2026	**Name of the Faculty:** Suchismita Satpathy, Asst.Prof. **Email ID: suchismita@cvrp.edu.in**
Subject: DIGITAL ELECTRONICS (ETCPC205)	**No. Of Days/Week:** 03	**Start Date: 01.07.2026** **End Date: 5.11.2026**

Week	Class Day	Theory Topics
1st	1st	**1.Logic Gates** Basic logic gates: OR, AND, and NOT
	2nd	Truth tables, Logic symbols
	3rd	Logic voltage levels ,Logic circuit design examples ,Integrated Circuits
2nd	1st	NOR, NAND, Exclusive OR, and Exclusive NOR gates. ,NOR and NAND gates used as inverters.
	2nd	Fan-in and fan-out, Termination of unused inputs ,AND and OR gates constructed from NAND and NOR gates.
	3rd	**Doubt clearing & Problem Solving class.**
3rd	1st	**2. Boolean Algebra** Boolean operations (OR, AND, NOT)
	2nd	Representation of logic circuits by Boolean expressions.,Laws of Boolean algebra: Double inversion: A"=A ,OR identities: A+0 = A, A+1=1, A+A=A, A+A'=1 ,AND identities: A.0=0, A.1=A, A.A=A, A.A'=0
	3rd	Cumulative laws: A+B=B+A, A.B=B.A ,Associative laws: (A+B)+C=A+(B+C), (A.B).C=A.(B.C) ,Distributive laws: A+(B.C)=(A+B).(A+C), A.(B+C)=A.B+A.C 2.3.7 De Morgan's theorems :(A+B+C+...)'=A'.B'.C'...,(A.B.C...)'=A'+B'+C'...
4th	1st	Applications to logic circuit simplifications and design, Equivalent logic gates, NAND and NOR implementations of logic circuits.
	2nd	Standard forms of Boolean expressions ,Sum-of-products (SOP) ,Product-of-sums (POS), Karnaugh mapping
	3rd	**Doubt clearing & Problem Solving class.**
5th	1st	**3. Combinational Logic Circuits:** Half adder **,**Full adder.
	2nd	Half Subtractor, Full Subtractor, 4 bit adder, Multiplexer (4:1).
	3rd	De- multiplexer (1:4) ,Decoder Encoder.
6th	1st	Digital comparator (3 Bit) ,Seven Segment Decoder

	2nd	**4. Latches & Flip-Flops:** Basic latches **,**NOR latch **,**NAND latch **,**Example uses of latches
	3rd	Gated latches ,Gated S-R latch ,Gated D-latch
7th	1st	Flip-flops: Master-slave and edge-triggered principles, S-R flip-flop.
	2nd	D-type flip-flop ,J-K flip-flop
	3rd	T-type flip-flop ,Flip-flop timing diagrams
8th	1st	**Doubt clearing & Problem Solving class.**
	2nd	**5. Counters :**Circuit diagramand working principle of Binary counters
	3rd	up-down counter (circuits, truth tables, and timing diagrams)
9th	1st	Asynchronous counters and ripple counter ,Synchronous counters
	2nd	Decade counter ,Module–n counter and its combinations
	3rd	Divide-by-n counters obtained from truncated binary sequences 5.8. Synchronous counter design using D-type flip-flops
10th	1st	Synchronous counter design using J-K flip-flops
	2nd	**Doubt clearing & Problem Solving class.**
	3rd	**6.Shift Registers :** Circuit diagram, truth tables, and timing diagrams of Shift Registers
11th	1st	Serial input shift register ,Serial/parallel load shift register
	2nd	Shift register counters,Ring counter
	3rd	Self-starting ring counter ,Johnson counter
12th	1st	**7.Semiconductor Memories :** Define the terms ROM, RAM, PROM, EPROM.
	2nd	Draw a typical memory cell :Design a small diode matrix ROM to serve as a code converter.
	3rd	Design and draw the logic diagram of a specified size memory system, Operating principle of dynamic memory
13th	1st	Advantages and disadvantages of dynamic memory vs. static memory ,Difference between dynamic memory vs. static memory
	2nd	**Doubt clearing & Problem Solving class.**
	3rd	**8. Sequential Circuit Design :**Combinational vs. Sequential circuits
14th	1st	Adder, Subtractor, decoder
	2nd	multiplexer, de-multiplexer, and comparator
	3rd	Finite state machines- Concept only
15th	1st	**Doubt clearing & Problem Solving class.**
	2nd	Previous Year Question Discussion.
	3rd	Previous Year Question Discussion.

Concerned Faculty **H.O.D.**