VLSI & EMBEDDED SYSTEM

5th SEMESTER-ETC

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UNIT-1
Introduction to VLSI & MOS Transistor

Historical Perspective

The electronics industry has achieved a phenomenal growth over the last few decades, mainly due to the rapid advances in integration technologies and large-scale systems design. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. Typically, the required computationaland informationprocessing power ofthese applications is the driving force for the fast development of this field. Figure 1 gives an overview of the prominent trends in informationtechnologiesoverthe next decade.The current leadingedge technologies(suchas low bit-rate video and cellular communications) already provide the end-users a certain amount of processing power and portability. This trend is expected to continue, with very important implications for VLSI and systems design. One of the most important characteristicsofinformationservices istheir increasing need for veryhighprocessing power and bandwidth (in order to handle real-time video, forexample).

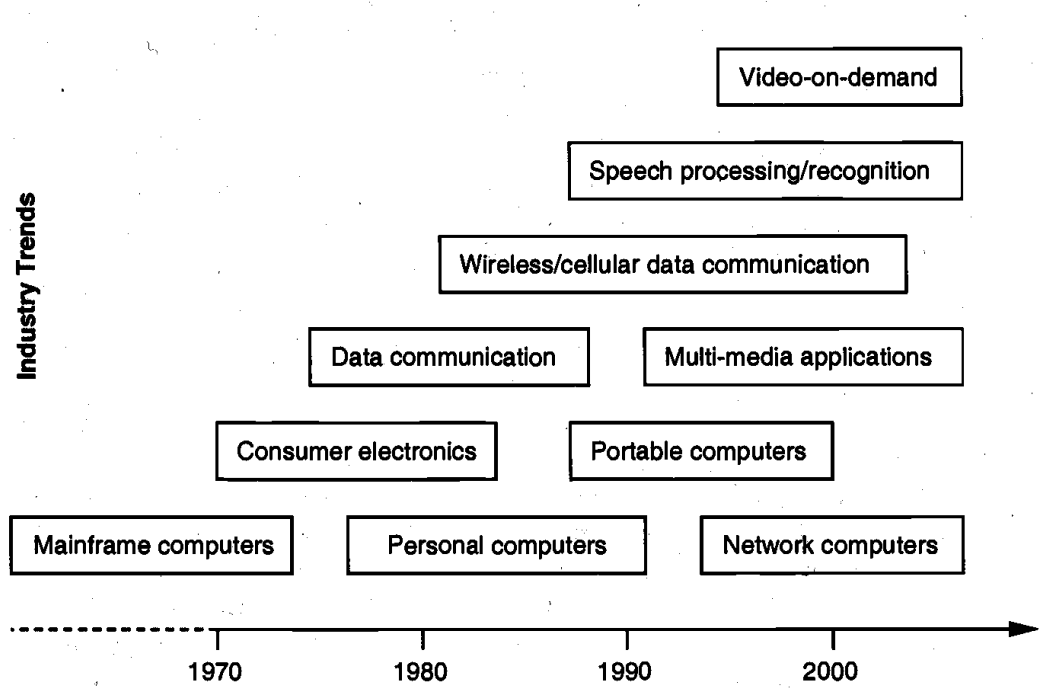


FIG.1(Prominent"driving"trendsininformationservicetechnologies.)

ERA	DATE	COMPLEXITY (# of logic blocks per chip)
Single transistor	1958	< 1
Unit logic (one gate)	1960	1
Multi-function	1962	2 - 4
Complex function	1964	5 - 20
Medium Scale Integration (MSI)	1967	20 - 200
Large Scale Integration (LSI)	1972	200 - 2,000
Very Large Scale Integration (VLSI)	1978	2,000 - 20,000
Ultra Large Scale Integration (ULSI)	1989	20,000 - ?

VLSIDESIGNMETHODOLOGIESANDVLSIDESIGNFLOW VLSI DESIGN METHODOLOGIES

The demands of the rapidly rising chip complexity has created significant challenges in many areas; practically hundreds of team members are involved in the development of a typical VLSI product, including the development of technology,computer-aideddesign (CAD) tools, chip design, fabrication, packaging, testing and reliability qualification. The level of circuit performance which can be reached within a certain design time strongly depends on the efficiency of the design methodologies, as well as on the design style two different VLSI design styles are compared for their relative merits in the design of the same product.

1. FULLCUSTOMDESIGN
2. SEMICUSTOM DESIGN

FULL CUSTOM DESIGN - Using the full-customdesignstyle (where the geometry and the placement of every transistor can be optimized individually) requires a longer time until design maturity can be reached, yet the inherent flexibility of adjusting almost every aspect of circuit design allows far more opportunity for circuit performance improvement during the design cycle. The final

product typically has a high level of performance (e.g. high processing speed, low power dissipation) and the silicon area is relatively small because of better area utilization. But this comes at a larger cost in terms of design time.

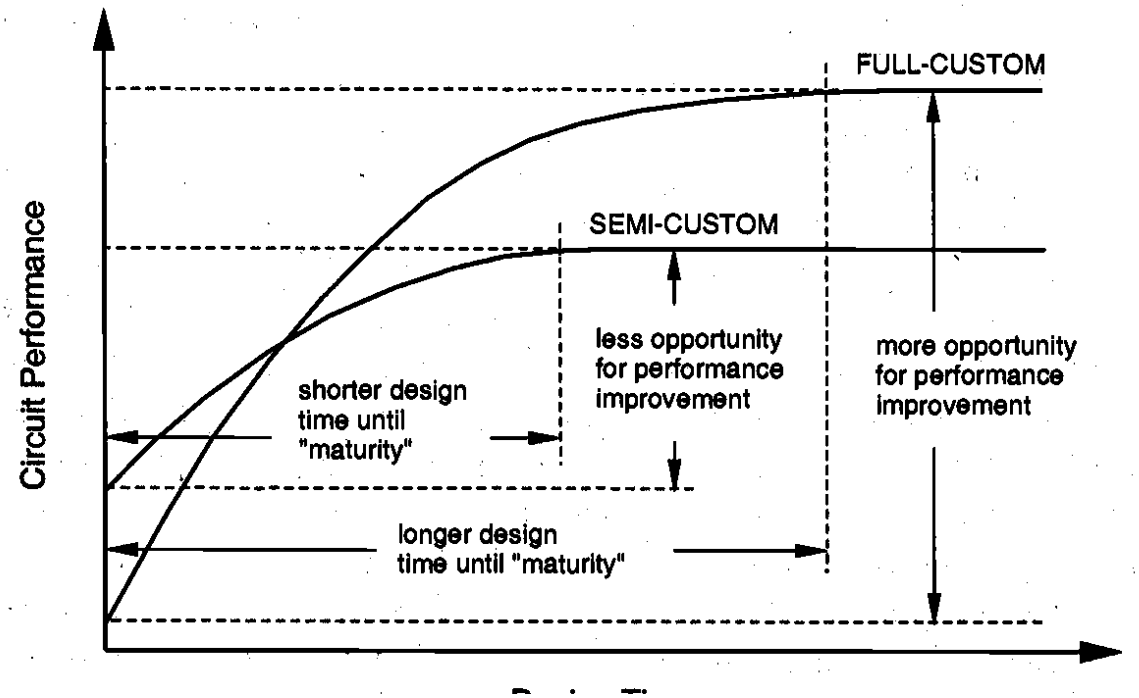


Figure-.2(ImpactofdifferentVLSIdesignstylesuponthedesigncycletimeandthe achievable circuit performance).

SEMI-CUSTOM DESIGN - Using a semi-custom design style (such asstandard- cell based design or FPGA) will allow a shorter design time until design maturity can be achieved. In the early design phase, the circuit performance can be even higher than that of a full-custom design, since some of the components used in semi-custom design are already optimized. But the semi-custom design style offers less opportunity for performance improvement over the long run, and the overall performance of the final product will inevitably be less than that of a full-customdesign.

In addition to the proper choice of a VLSI design style, there are other issues which must be addressed in view of the constantly evolving nature of the VLSI manufacturing technologies. Approximately every two years, a new generation of technology is introduced, which typically allows for smaller device dimensions and consequently, higher integration density and higher performance.

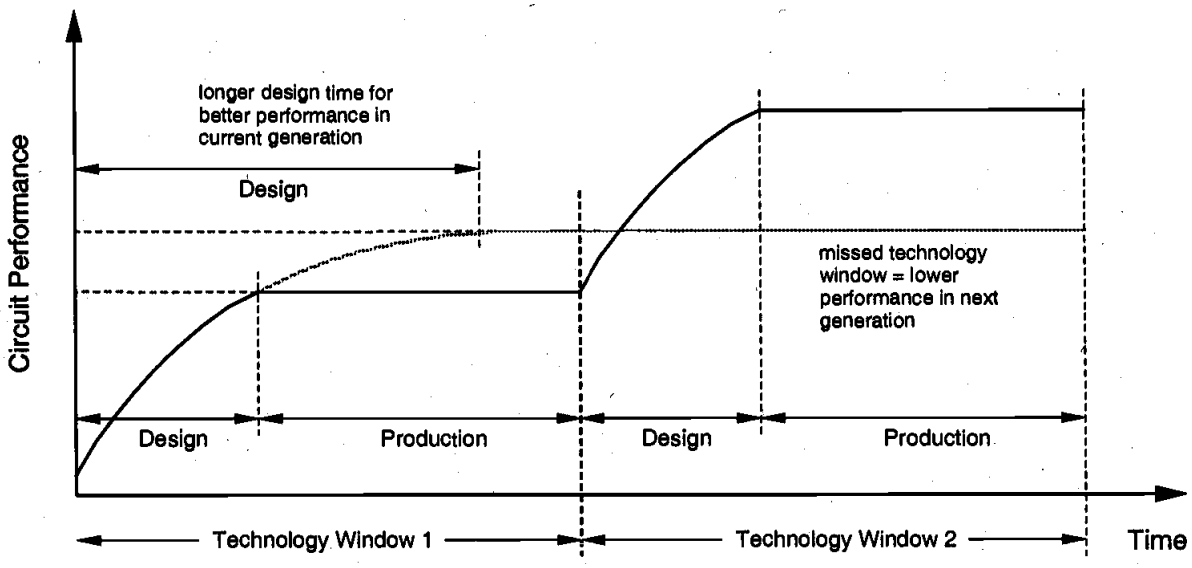


Figure3. (ProgressiveperformanceimprovementofaVLSIproduct)

VLSIDesign Flow

The designprocess, at various levels, is usuallyevolutionaryin nature. It starts witha given set of requirements. Initial design is developed and tested against the requirements. Whenrequirements are not met, the design has tobe improved. Ifsuch improvement is either not possible or too costly, then a revision of requirements and an impact analysis must be considered. The Y-chart (first introduced by D. Gajski) shown in Fig. 4 illustrates a design flow for most logic chips, using design activities on three different axes (domains) which resemble the letter "Y."

The Y-chart consists of three domains of representation, namely (i) behavioural domain, (ii) structural domain, and (iii) geometrical layout domain. The design flow starts from the algorithm that describes the behavior of the target chip. The corresponding architecture of the processor is first defined. It is mapped onto the chip surface by floorplanning. The next design evolution in the behavioral domain defines finite state machines (FSMs) which are structurally implemented with functional modules such as registers and arithmetic logic units (ALUs). Thesemodules are then geometrically placed onto the chip surface using CAD tools for automatic module placement followed by routing, with a goal of minimizing the interconnects area and signal delays. The third evolution starts with a behavioral module description. Individual modules are then implemented with leaf cells. At this stage the chip is described in terms of logic gates (leaf cells), which can be placed and interconnected byusing a cellplacement and routing program.

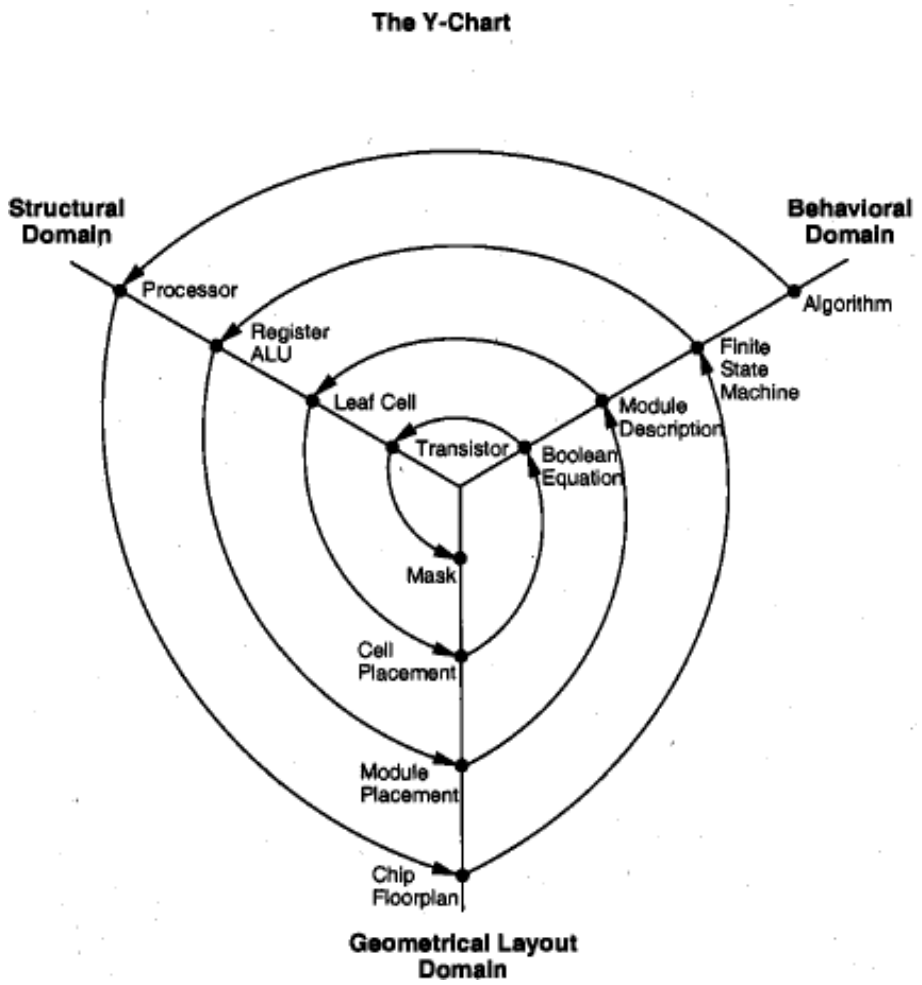


Figure4.3.TypicalVLSIdesignflow inthreedomains(Y-chartrepresentation).

The last evolution involves a detailed Boolean description of leaf cells followed by a transistor level implementation of leaf cells and mask generation. In the standardcell based designstyle, leafcells arepredesigned(atthetransistor level) andstoredina libraryfor logic implementation, effectively eliminating the need for the transistor level design. Figure 4 provides a more simplified view of the VLSI design flow, taking into account the various representations, or abstractions of design: behavioral, logic, circuit and masklayout. Notethat the verification of design plays a very important role in every step during this process. The failure to properly verify a design in its early phases typically causes significant and expensive re-design at a later stage, which ultimately increases the time-to-market.

DesignHierarchy,DesignStyles&CADTechnology.

DesignHierarchy

The use of the hierarchy, or "divide and conquer" technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable. This approach is very similar to software development wherein large programsare split into smaller and smaller sectionsuntil simple subroutines, withwell-defined functions and interfaces, canbe written. Inthe physical domain, partitioning a complex system into its various functional blocks will provide a valuable guide for the actual realization of these blocks on the chip.

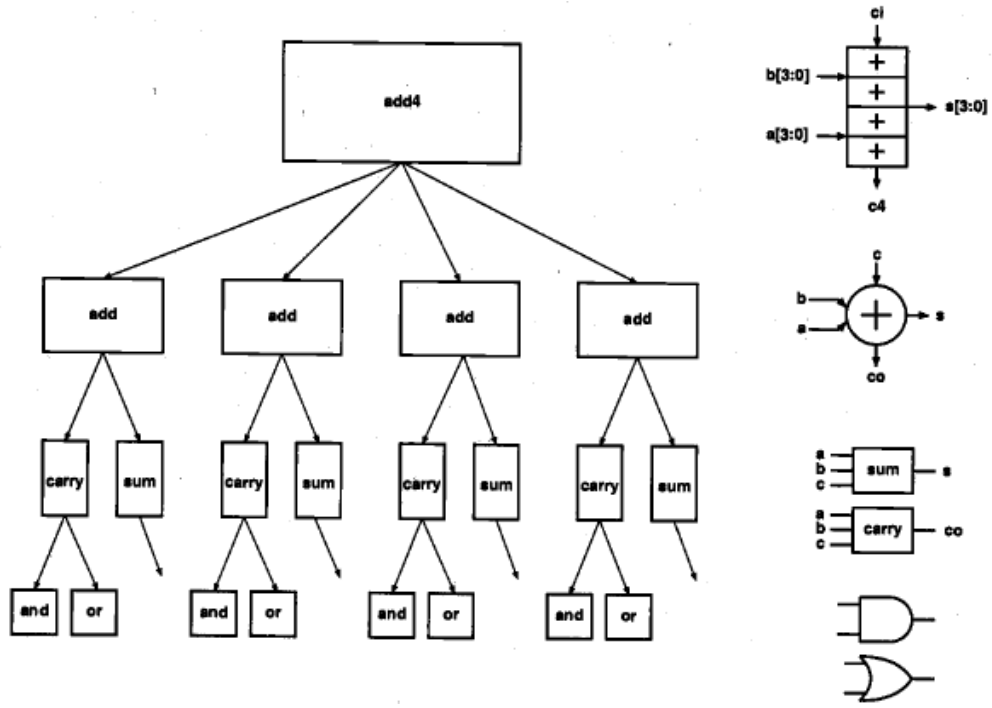


FIG-5(Structuraldecompositionofa4-bit adder, showingthelevelsofhierarchy).

Regularity,ModularityandLocality

Regularity means that the hierarchical decomposition of a large system should result in notonlysimple, but also similar blocks, as muchaspossible. Agoodexampleofregularity is the design ofarray structures consisting of identical cells - such as a parallel multiplication array.

Modularity indesign means that the various functionalblocks which make up the largersystemmust have *well-definedfunctions*and*interfaces.*Modularityallowsthat each

block or module can be designed relatively independently from each other, since there is no ambiguityabout the function and the signal interface ofthese blocks.

Locality also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible. This last point isextremely important for avoiding long interconnect delays

Computer-AidedDesignTechnology

CHAPTER 14 Computer-aided design (CAD) tools are essential for timely development of integrated circuits. Although CAD tools cannot replace the creative and inventive parts of the design activities, the majority of time-consuming and computation intensive mechanistic parts of the design can be executed by using CAD tools. The CAD technology for VLSI chip design can be categorized into the following areas:

* Highlevelsynthesis
* Logicsynthesis
* Circuitoptimization
* Layout
* Simulation
* Designruleschecking

SynthesisTools

The high-level synthesis tools using hardware description languages (HDLs), such as VHDL or Verilog, address the automation of the design phase in the top level of the design hierarchy.

Layout*Tools*

The tools for circuit optimization are concerned with transistor sizingfor minimization of delays and with process variations, noise, and reliability hazards. The layout CAD tools include floorplanning, place-and-route and module generation. Sophisticated layout tools are goaldriven and include some degree of optimization functions.

SimulationandVerificationTools

The simulationcategory, which isthe most mature areaofVLSI CAD, includes many tools ranging from circuit-level simulation (SPICE or its derivatives,such as HSPICE), timing level simulation, logic level simulation, and behavioral simulation. Many other simulationtools have also beendeveloped for device-levelsimulationand process simulation for technology development. The aim of all simulation CAD tools is to determine if the designed circuitmeetsthe required specifications, at allstages ofthe design process**.**

1.1:MOSTransistor

4.1.TheMetalOxideSemiconductor(MOS)Structure

We will start our investigation by considering the electrical behavior of the simple two-. terminal MOS structure shown in Fig. 3.1. Note that the structure consists of three layers: The metal gate electrode, the insulating oxide (SiO2) layer, and the p-type bulk semiconductor (Si), called the substrate. As such, the MOS structure forms a capacitor, with the gate and the substrate acting as the two terminals (plates) and the oxide layer as the dielectric. The thickness of the silicon dioxidelayeris usually between 10 nm and 50 nm. The carrier concentration andits local distribution within the semiconductor substrate can now be manipulated by the external voltages applied to the gate and substrate terminals. A basic understanding of the bias conditions for establishing different carrier concentrations in the substrate will also provide valuable insight into the operating conditions of more complicated MOSFET structures.

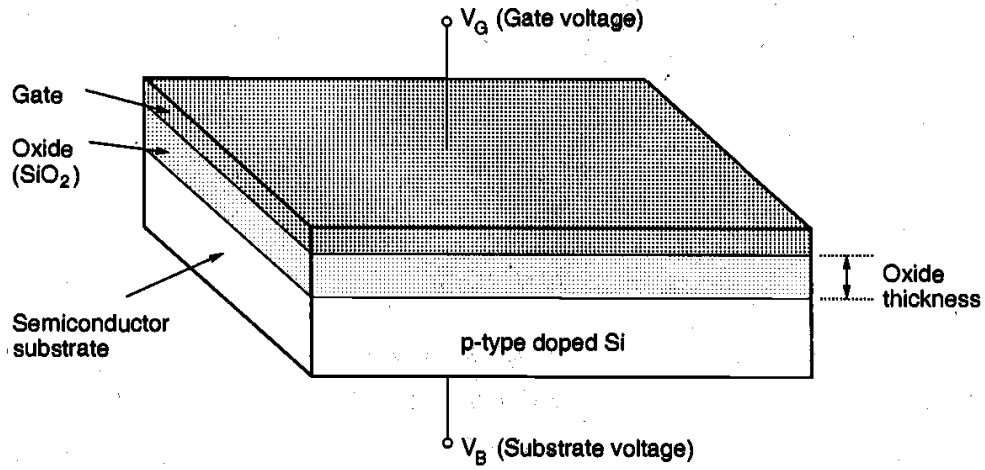


Figure 3.1. Two-terminal MOS structure.

Consider firstthebasicelectricalpropertiesofthesemiconductor(Si) substrate,which acts as one of/the electrodesofthe MOS capacitor. The equilibrium concentrations of mobile carriers in a semiconductor always obeythe *Mass Action Law*given by

$$n \cdot p = n_i^2 \qquad (3.1)$$

Here, *n* and p denote the mobile carrier concentrations of electrons and holes, respectively, and $n_i$denotesthe intrinsic carrier concentration ofsilicon, which is a function

ofthe temperature T. Atroomtemperature,i.e.,*T*= 300 K,*ni*is approximately equal to1.45 x 1010 cm-3. Assuming that the substrate is uniformly doped with an acceptor (e.g., Boron) concentration *NA*, the equilibriumelectronand hole concentrations in the p-type substrate are approximated by

$$n_{po} \cong \frac{n_i^2}{N_A}$$
$$p_{po} \cong N_A \qquad (3.2)$$

ThedopingconcentrationNA istypicallyontheorderof1015to1016cm-3;thus, it is much

greater than the intrinsic carrier concentration n_i

TheMOSSystemunderExternalBias

We now turn our attention to the electrical behavior of the MOS structure under externally applied bias voltages. Assume that the substrate voltage is setat VB = 0, andlet thegatevoltagebethecontrolling parameter. Depending onthepolarityand the magnitudeof VG, three different operating regions can be observed for the MOS system: accumulation, depletion, and inversion. Ifa negative voltageVGisappliedtothegateelectrode,theholes in the p-type substrate are attracted to the semiconductor-oxide interface. The majority carrier concentration near the surface becomes larger than the equilibrium hole concentration in the substrate; hence, this condition is called carrier accumulation on the surface (Fig. 3.5). Note that in this case, the oxide electric field is directed towards the gate electrode. The negative surface potentialalso causes the energy bands to bend upward near the surface.

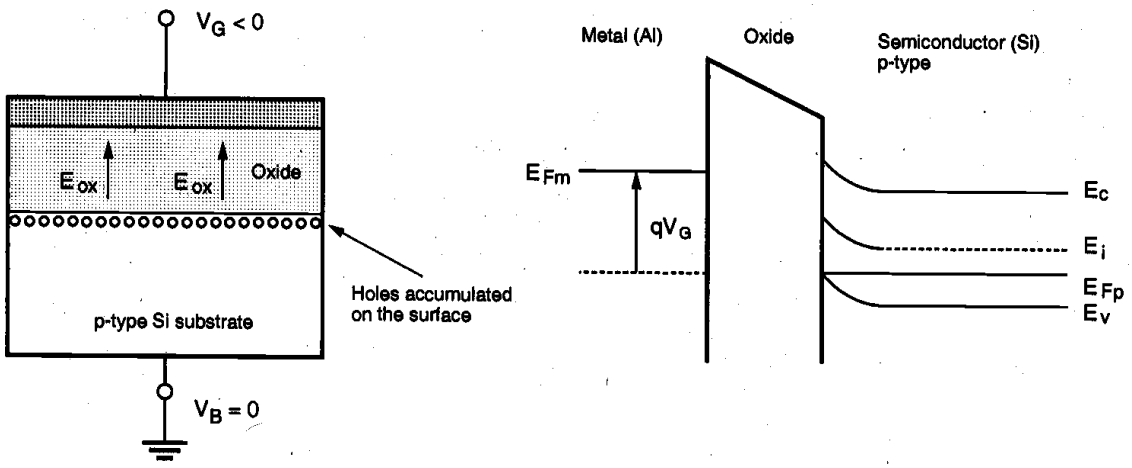
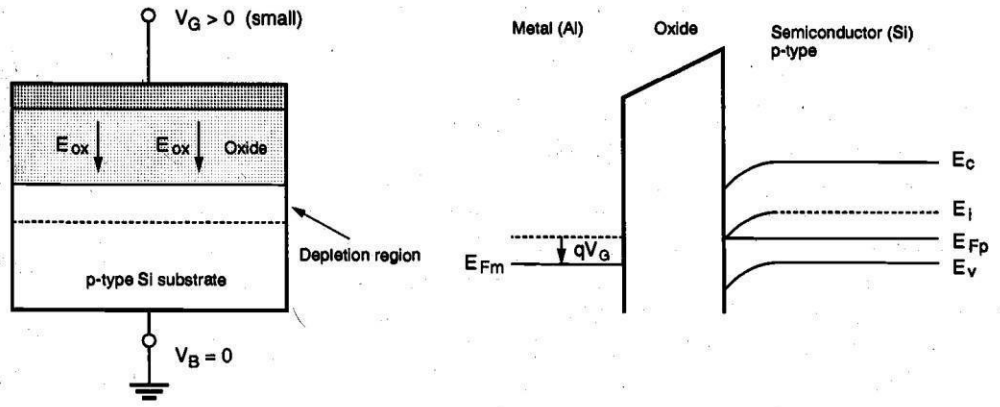


*Figure3.5.*The cross-sectionalview andtheenergyband diagramoftheMOSstructure

While the hole density near the surface increases as a result of the applied negative gate bias, the electron (minority carrier) concentration decreases as the negatively charged electrons are pushed deeper into the substrateoperating in accumulation region.



$$dQ = -q \cdot N_A \cdot dx \tag{3.7}$$

The *change* in surface potential required to displace this charge sheet dQ by a distance x_d away from the surface can be found by using the Poisson equation.

$$d\phi_s = -x \cdot \frac{dQ}{\varepsilon_{Si}} = \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} dx \tag{3.8}$$

Integrating (3.7) along the vertical dimension (perpendicular to the surface) yields

$$\int_{\phi_F}^{\phi_s} d\phi_s = \int_0^{x_d} \frac{q \cdot N_A \cdot x}{\varepsilon_{Si}} \, dx \tag{3.9}$$

$$\phi_s - \phi_F = \frac{q \cdot N_A \cdot x_d^2}{2\,\varepsilon_{Si}} \tag{3.10}$$

Thus, the depth of the depletion region is

$$x_d = \sqrt{\frac{2\varepsilon_{Si} \cdot |\phi_s - \phi_F|}{q \cdot N_A}} \tag{3.11}$$

and the depletion region charge density, which consists solely of fixed acceptor ions in this region, is given by the following expression

$$Q = -q \cdot N_A \cdot x_d = -\sqrt{2q \cdot N_A \cdot \varepsilon_{Si} \cdot |\phi_s - \phi_F|} \tag{3.12}$$

Now consider the next case in which a small positive gate bias VG is applied to the gate electrode. Since the substrate bias is zero, the oxide electric fieldwill be directedtowards the substrate in this case. The positive surface potential causes the energy bands to bend downward near the surface, as shown in Fig. 3.6. The majoritycarriers, i.e., the holes in the substrate, will be repelled back into the substrate as a result of the positive gate bias, and these holes willleave negativelycharged fixed acceptorions behind. Thus, a depletionregion is created near the surface. Note that under this bias condition, the region near the semiconductor-oxide interface is nearlydevoid of all mobile carriers.

To complete our qualitative overview of different bias conditions and their effects upontheMOSsystem, consider next a further increase in thepositivegatebias. Asaresult of the increasing surface potential, the downward bending of the energy bands will increase as well. Eventually, the mid-gap energy level Ei becomes smaller than the Fermi level EFP on the surface, which means that the substrate semiconductor in this region becomes n-type. Within this thin layer, the electron density is larger than the majority hole density, since the positive gate potential attracts additional minority carriers (electrons) from the bulk substrate to the surface (Fig. 3.7).

$$x_{dm} = \sqrt{\frac{2 \cdot \varepsilon_{Si} \cdot |2\phi_F|}{q \cdot N_A}} \qquad (3.13)$$

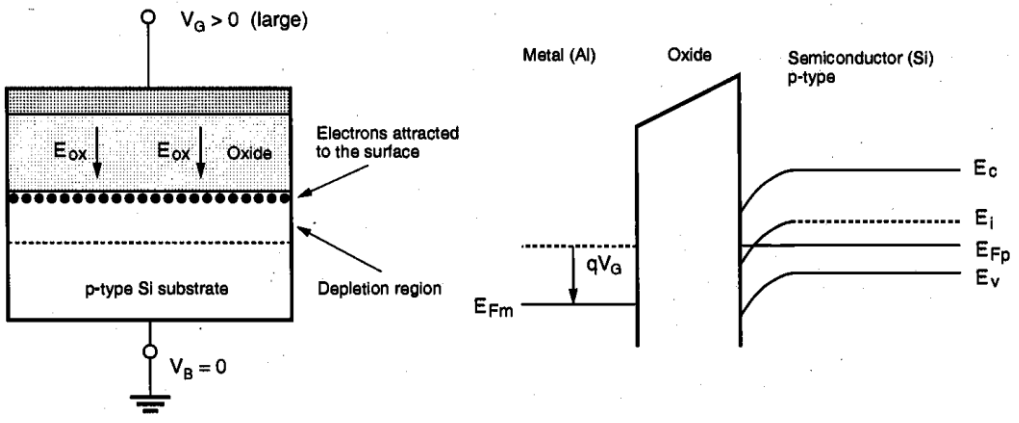


Figure 3.7. The cross-sectional view and the energy band diagram of the MOS structure in surface inversion, under larger gate bias voltage.

The n-type region created near the surface by the positive gate bias is called the inversion layer, and this condition is called surface inversion. It will be seen that the thin inversion layer on the surface with a large mobile electron concentration can be utilized for conducting current between two terminals of the MOS transistor. The creation ofa conducting surface inversion layer through externally applied gate bias is an essential phenomenon for current conduction inMOS transistors. Inthe following we willexamine the structure and the operation of the MOS Field Effect Transistor (MOSFET).

MOSFETCurrent-VoltageCharacteristics

The analytical derivation of the MOSFET current-voltage relationships for various bias conditions requires that severalapproximations be made to simplify the problem.

Without these simplifying assumptions, analysis of the actualthree-dimensionalMOS system would become a very complex task and would prevent the derivation of closed form current-voltage equations. In the' following, we will use the *gradual channel approximation* (GCA) for establishing the MOSFET current-voltage relationships, whichwill effectivelyreduce the analysis to a one-dimensionalcurrent-flow problem. This will allow us to devise relatively simple current equations that agree well with experimental results. As in every approximate approach, however, the GCA also has its limitations, especially for small-geometry MOSFETs. We will investigate the most significant limitations and examine some of the possible remedies.

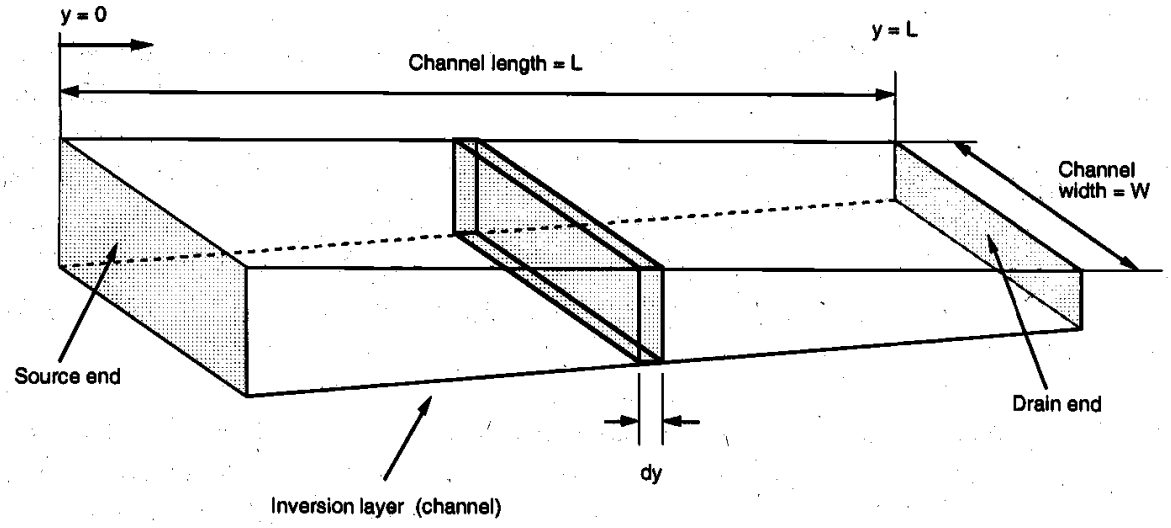


Figure 3.16. **Simplified geometry of the surface inversion layer (channel region).**

Now consider the incremental resistance *dR* of the differential channelsegment shown inFig. 3.16. Assuming that all mobile electrons inthe inversion layer have a constant

*surfacemobility*jun,the incrementalresistancecanbeexpressedas follows. Notethatthe minus sign is due to the negative polarityofthe inversion layer charge Q_I.

$$dR = -\frac{dy}{W \cdot \mu_n \cdot Q_I(y)} \quad \text{.....(1)}$$

The *electron surface mobility yun* used , depends on the doping concentration of the channel region, and its magnitude is typically about one-half of that of the bulk electron mobility. We will assume that the channel current density is uniform across this segment. According to our one-dimensional model, the channel (drain) current *ID* flows between the source and the drain regions in the y-coordinate direction. Applying Ohm's law for this segment yields the voltage dropalong the incrementalsegment *dy*, inthe ydirection.

$$dV_c = I_D \cdot dR = -\frac{I_D}{W \cdot \mu_n \cdot Q_I(y)} \cdot dy \quad \text{.....(2)}$$

Thisequationcannowbe integratedalongthechannel, i.e., fromy=0to y=L, using the

boundary conditions given in above equation

$$\int_0^L I_D \cdot dy = -W \cdot \mu_n \int_0^{V_{DS}} Q_I(y) \cdot dV_c \quad \text{.....(3)}$$

The left-hand sideofthis equation issimplyequalto LID.Theintegralontheright- hand side is evaluated by replacing $Q_I$in

$Q_I(y)$=-Cox[VGS vVC(Y)-VTO]

$$I_D = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2\right] \quad \text{.....(4)}$$

Equation(3.32) representsthe draincurrent ID asa simple second-order function of the

twoexternalvoltages,VGS andVDS.Thiscurrent equationcanalso berewrittenas

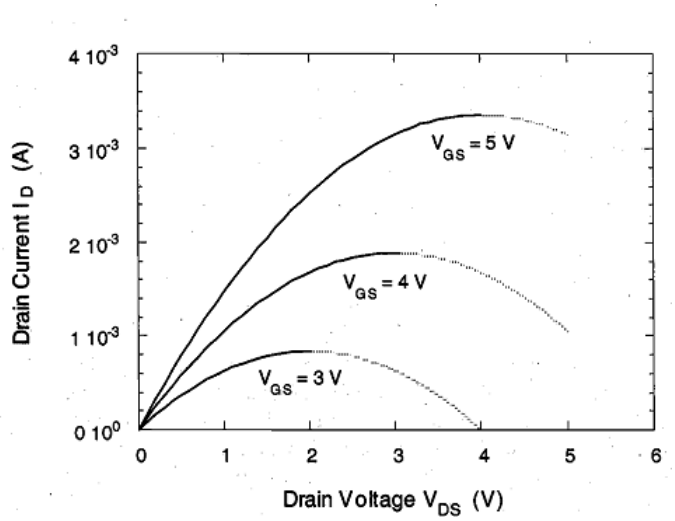
$$I_D = \frac{k}{2} \cdot \left[2 \cdot (V_{GS} - V_{T0}) V_{DS} - V_{DS}^2\right] \quad \text{.....(5)}$$

wheretheparameterskandk'aredefinedas

$$k' = \mu_n \cdot C_{ox}$$

$$k = k' \cdot \frac{W}{L} \quad \text{..... (6)}$$

The drain current equation given in (5)is the simplestanalytical approximation for the MOSFET current-voltage relationship. Note that, in addition to the process dependent constants k' and V,the current-voltage relationship is also affected bythe device dimensions, W and L. In fact, we will see that the ratio of WIL is one of the most important design parameters in MOS digital circuit design. Now, we must determine the region of validity for this equation and what this means for the practical use ofthe equation.



The draincurrent-drain voltage curves shownabove reachtheir peak value for VDS = V_{GS} - V_{TO} Beyond this maximum, each curve exhibits a negative differential conductance, which is not observed in actual MOSFET current-voltage measurements (section shown by the dashed lines). We must remember now that the drain currentequation (4) has been derived under the following voltage assumptions,

$$V_{GS} \geq V_{T0}$$
$$V_{GD} = V_{GS} - V_{DS} \geq V_{T0}$$

$$V_{DS} \geq V_{DSAT} = V_{GS} - V_{T0} \quad \text{..... (7)}$$

Also, drain current measurements with constant V_S show that the current I_D does not show much variation as a function of the drain voltage. V_{DS} beyond the saturation boundary, but rather remains approximately constant around the peak value reached for V_{DS} = VD_{SAT}This saturation drain current levelcan be found simply bysubstituting (7) for VDS in (1

$$I_D(sat) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot \left[2 \cdot (V_{GS} - V_{T0}) \cdot (V_{GS} - V_{T0}) - (V_{GS} - V_{T0})^2\right]$$

$$= \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_{T0})^2$$

..... (8)

Thus, the drain current ID becomes afunction only of the gate-to-source voltage VGS, beyond the saturation boundary. Note that this constant saturation current approximation is not very accurate in reality, and that the saturation-region drain current continues to have a certain dependence on the drain voltage. For simple hand calculations, however,(8) provides a sufficiently accurate approximation of the MOSFET drain (channel) current in saturation.

MOSFETscalingandsmallgeometryeffects.

MOSFET Scaling and Small-Geometry Effects The design of high-density chips in MOS VLSI (Very Large Scale Integration) technology requires that the packing density of MOSFETs used in the circuits is as high as possible and, consequently, that the sizes of the transistors are as small as possible. The reduction of the size, i.e., the dimensions of MOSFETs, is commonly referred to as scaling.

There aretwo basic types ofsize-reductionstrategies:

fullscaling(also calledconstant-fieldscaling)

constant voltagescaling.

FullScaling(Constant-FieldScaling)

This scaling optionattempts to preserve the magnitudeof internalelectric fields inthe MOSFET, while the dimensions are scaled down by a factor of S. To achieve this goal, all potentials must be scaled down proportionally, by the same scaling factor. Note that this potential scaling also affects the threshold voltage V_{TO}Finally, the Poisson equation describing the relationship between charge densities and electric fieldsdictates thatthe charge densities must be increased by a factor of S in order to maintain the field conditions. Table 1 liststhe scaling factorsforallsignificant dimensions, potentials, and doping densities of the MOS transistor.

Quantity	Before Scaling	After Scaling
Channel length	L	$L' = L / S$
Channel width	W	$W' = W / S$
Gate oxide thickness	t_{ox}	$t_{ox}' = t_{ox} / S$
Junction depth	x_j	$x_j' = x_j / S$
Power supply voltage	V_{DD}	$V_{DD}' = V_{DD} / S$
Threshold voltage	V_{T0}	$V_{T0}' = V_{T0} / S$
Doping densities	N_A N_D	$N_A' = S \cdot N_A$ $N_D' = S \cdot N_D$

Table1. FullscalingofMOSFET dimensions,potentials, anddopingdensities.

Constant-VoltageScaling

While the full scaling strategy dictates that the power supply voltage and all terminal voltages be scaled down proportionally with the device dimensions, the scaling of voltages may not be very practical in many cases. In particular, the peripheral and interface circuitry may require certain voltage levels for all input and output voltages, which in turn would necessitate multiple power supply voltages and complicated level shifter arrangements. For these reasons, constant-voltage scaling is usuallypreferred over full scaling.

Quantity	Before Scaling	After Scaling
Oxide capacitance	C_{ox}	$C_{ox}' = S \cdot C_{ox}$
Drain current	I_D	$I_D' = I_D / S$
Power dissipation	P	$P' = P / S^2$
Power density	$P / Area$	$P' / Area' = P / Area$

Table2.Effectsoffullscaluponkeydevicecharacteristics.

ExplainMOSFETcapacitances.

The majority of the topics covered in this chapter has been related to the steady-state behavior ofthe MOS transistor. The current-voltage characteristics investigated here can be

applied for investigating the DC response of MOS circuits under variousoperating conditions.

the gate electrode overlaps both the source region and the drain region at the edges. The two overlap capacitances that arise as a result of this structural arrangement are called CGD (overlap) and CGS (overlap), respectively. Assuming that boththe source and the drain diffusion regions have the same width W, the overlap capacitances can be found as

$$C_{GS}(overlap) = C_{ox} \cdot W \cdot L_D$$
$$C_{GD}(overlap) = C_{ox} \cdot W \cdot L_D$$

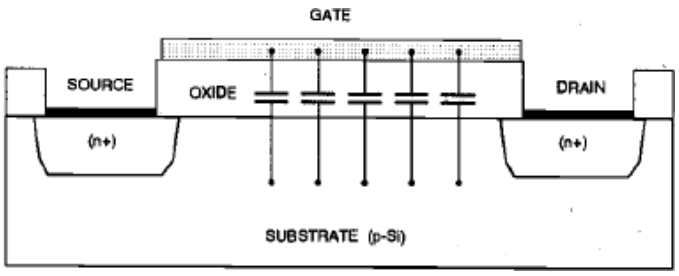
$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

Note that both of these overlap capacitances do not depend on the bias conditions, i.e., they are voltage-independent. Now consider the capacitances which result from the interaction between the gate voltage and the channel charge.Since the channel region is connected to the source, the drain, and the substrate, we can identify three capacitances between the gate and these regions, i.e., Cgs, C d and C b respectively. Notice that inreality, the gate-to-channelcapacitance isdistributed and voltage-dependent. Then, the gate-to-source capacitance Cgs is actually the gate-to-channel capacitance seen between the gate and the source terminals; the gate-to-drain capacitance C ad is actually the gate-to-channelcapacitance seen between the gate and the drain terminals. Asimplified view oftheir bias-dependence can be obtained by observing the conditions in the channel region duringcut-off, linear, and saturation modes.

In cut-off mode (Fig. (a)), the surface is not inverted. Consequently, there is no conducting channel that links the surface to the source and to the drain. Therefore, the gate-to-source and the gate-to-drain capacitances are both equal to zero: Cgs = Cgd= 0. The gate-to-substrate capacitance can be approximated by

$$C_{gb} = C_{ox} \cdot W \cdot L$$

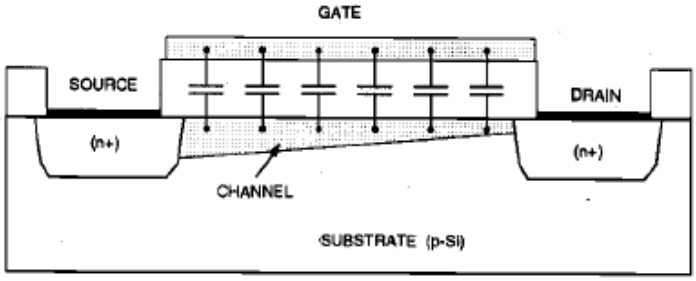
(a)



In linear-mode operation, the inverted channel extends across the MOSFET, between the source and the drain (Fig. (b)). This conducting inversion layer on the surface effectively shields the substrate from the gate electric field; thus, Cgb = 0. In this case, the distributed gate-to-channel capacitance may be viewed as being shared equally between the source and the drain, yielding

$$C_{gs} \cong C_{gd} \cong \frac{1}{2} \cdot C_{ox} \cdot W \cdot L$$

(b)



Whenthe MOSFET isoperating insaturation mode,the inversion layer onthe surface does not extend to the drain, but it is pinched off (Fig. (c)). The gate-to-drain cca pacitance component is therefore equal to zero (Cgd = 0) . Since the source is still linked to the conducting channel, its shielding effect also forces the gate-to-substrate capacitance to be zero, Cgb = 0. Finally, the distributed gate-to-channel capacitance as seen between the gate and the source can be approximated by

$$C_{gs} \cong \frac{2}{3} \cdot C_{ox} \cdot W \cdot L$$

(c)

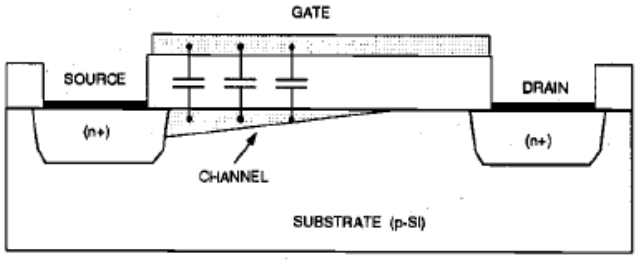


Figure..SchematicrepresentationofMOSFETоxidecapacitancesduring(a)cut-off,(b) linear, and (c) saturation modes.

Capacitance	Cut-off	Linear	Saturation
C_{gb} (total)	$C_{ox}WL$	0	0
C_{gd} (total)	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$C_{ox}WL_D$
C_{gs} (total)	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$\frac{2}{3}C_{ox}WL + C_{ox}WL_D$

TableforApproximateoxidecapacitancevaluesforthreeoperatingmodesoftheMOS

ModelingofMOSTransistorsincludingBasic conceptsoftheSPICElevel-1models.thelevel-2 and level-3 model

TheLEVEL1 ModelEquations

The LEVEL 1 model is the simplest current-voltage description of the MOSFET, which is basically the GCA-based quadratic model originally proposed by Shichman and Hodges. The equations used for the LEVEL 1 n-channel MOSFET model in SPICE are as follows.

Linear Region

$$I_D = \frac{k'}{2}\cdot\frac{W}{L_{eff}}\cdot\left[2\cdot(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]\cdot(1+\lambda V_{DS}) \quad \text{for} \quad V_{GS}\geq V_T$$

$$\text{and} \quad V_{DS} < V_{GS}-V_T \qquad \text{.....(1)}$$

Saturation Region

$$I_D = \frac{k'}{2}\cdot\frac{W}{L_{eff}}\cdot(V_{GS}-V_T)^2\cdot(1+\lambda\cdot V_{DS}) \qquad \text{for} \quad V_{GS}\geq V_T$$

$$\text{and} \quad V_{DS}\geq V_{GS}-V_T$$

wherethethresholdvoltage$V_T$iscalculated as

$$V_T = V_{T0}+\gamma\cdot\left(\sqrt{|2\phi_F|+V_{SB}}-\sqrt{|2\phi_F|}\right)$$

Notethattheeffectivechannellength$L_e$usedintheseequationsisfoundasfollows:

$$L_{eff} = L-2\cdot L_D$$

TheLEVEL2 ModelEquations

To obtain a more accurate model for the drain current, it is necessary to eliminate some of the simplifying assumptions made in the original GCA analysis. Specifically,the bulk depletion charge must be calculated by taking into accountits dependence on the channel voltage. Solving the drain current equation using the voltage-dependent bulk charge term, the following current-voltage characteristics can be obtained:

$$I_D = \frac{k'}{(1-\lambda\cdot V_{DS})}\cdot\frac{W}{L_{eff}}\cdot\left\{\left(V_{GS}-V_{FB}-|2\phi_F|-\frac{V_{DS}}{2}\right)\cdot V_{DS}\right.$$
$$\left.-\frac{2}{3}\cdot\gamma\cdot\left[(V_{DS}-V_{BS}+|2\phi_F|)^{3/2}-(-V_{BS}+|2\phi_F|)^{3/2}\right]\right\}$$

thesaturationvoltageV_{DSAT}canbecalculatedas

$$V_{DSAT} = V_{GS} - V_{FB} - |2\phi_F| + \gamma^2 \cdot \left(1 - \sqrt{1 + \frac{2}{\gamma^2} \cdot (V_{GS} - V_{FB})}\right)$$

Thesaturationmodecurrentis

$$I_D = I_{Dsat} \cdot \frac{1}{(1 - \lambda \cdot V_{DS})}$$

TheLEVEL3 ModelEquations

The LEVEL 3 model has been developed for simulation of short-channel MOS' transistors; it can represent the characteristics of MOSFETs quite precisely forchannel lengths down to 2 gum. The current-voltage equations are formulated in the same way as for the LEVEL 2 model.

$$I_D = \mu_s \cdot C_{ox} \cdot \frac{W}{L_{eff}} \cdot \left(V_{GS} - V_T - \frac{1 + F_B}{2} \cdot V_{DS}\right) \cdot V_{DS}$$

Where

$$F_B = \frac{\gamma \cdot F_s}{4 \cdot \sqrt{|2\phi_F| + V_{SB}}} + F_n$$

Theempiricalparameter*FB*expressesthedependenceofthebulkdepletionchargeon the

three-dimensionalgeometryoftheMOSFET.Here,theparameters*VT*,*Fs*,and *u*sare influenced by the short-channel effects, while the parameter Fn is influenced by the narrow-channeleffects. The dependence ofthe surface mobilityon the gate electric field is simulated as follows:

$$\mu_s = \frac{\mu}{1 + \theta \cdot (V_{GS} - V_T)}$$

UNIT-2
FABRICATIONOFMOSFETS

ExplainFabricationprocesses(NMOSFabrication,CMOSn-wellprocess)

FABRICATION PROCESS

Theprocessstartswiththecreationofthen-wellregionsforpMOStransistors,by impurity implantation into the substrate. Then, a thick oxide is grown in the regions surrounding the nMOS and pMOS active regions. The thin gate oxide is subsequentlygrown on the surface through thermal oxidation. These steps are followed by the creation of n+ and p+ regions (source, drain, and channel stop implants) and by final metallization (creation of metal interconnects).

Each processing step requires that certain areas are defined on chip by appropriate masks.As a result patterned layers of doped silicon, polysilicon, metal, and insulating silicon dioxide. In general, a layer must be patterned before the next layer of material is applied on the chip. The process used to transfer a pattern to a layer on the chip is called *lithography*. Since each layer has its own distinct patterning requirements, the lithographic sequence must be repeated for every layer, using a different mask.

starts with the thermal oxidation of the silicon surface, by which an oxide layer of about 1 m thickness, for example, is created on the substrate (Fig. (b)). The entire oxide surface is then covered with a layer of photo-resist, which is essentially a light-sensitive,acid-resistant organic polymer, initially insoluble in the developing solution (Fig.(c)).

If the photo-resist material is exposed to ultraviolet (UV) light, the exposed areas become soluble so that theyare no longer resistant to etching solvents. To selectively expose the photo-resist, we have to cover some of the areas on the surface with a mask during exposure. Thus, when the structure with the mask ontop is exposed to UV light, areas which are covered bythe opaque features onthe mask are shielded. Inthe areas where the UV light can pass through, on the other hand, the photo-resist is exposed and becomes soluble (Fig. (d)).

The type of photo-resist which is initially insoluble and becomes soluble after exposure to UV light is called *positive photo-resist.*

There is another type of photo-resist which is initially soluble and becomes insoluble (hardened) after exposure to UV light, called negative photo-resist. Ifnegative photo-resist is used in the photolithography process,

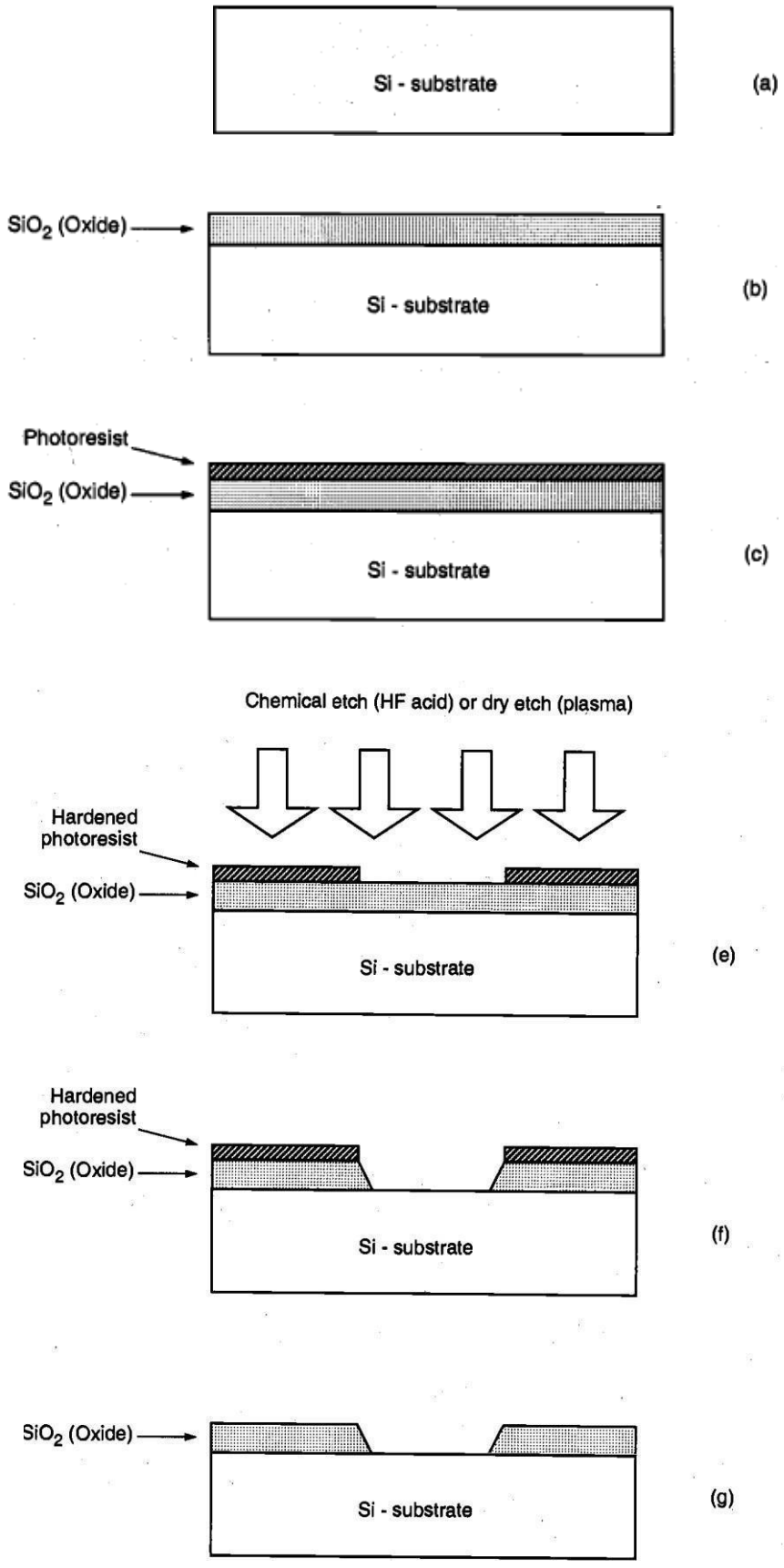


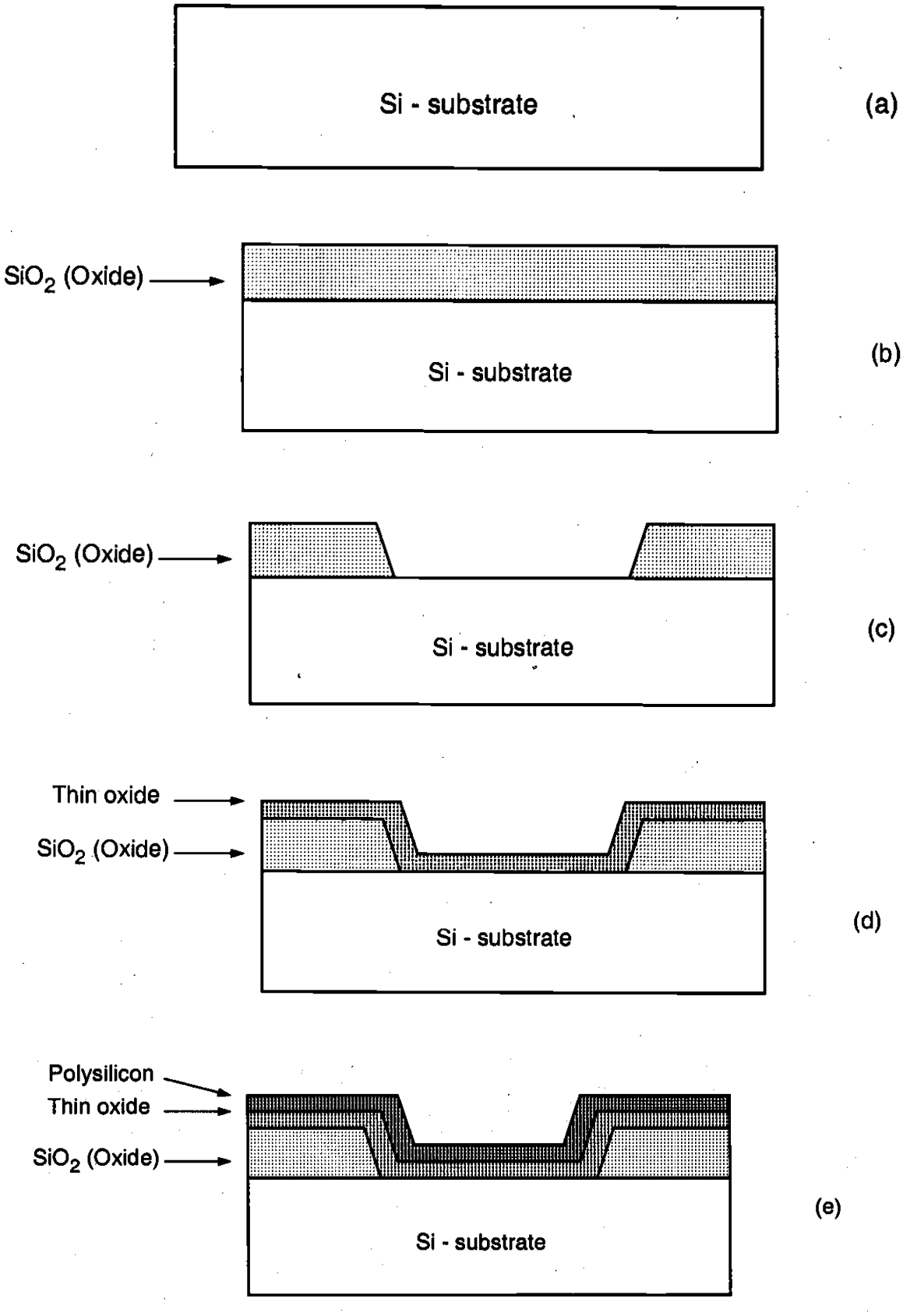
FIG-Processstepsrequiredfor patterningofsilicondioxide.

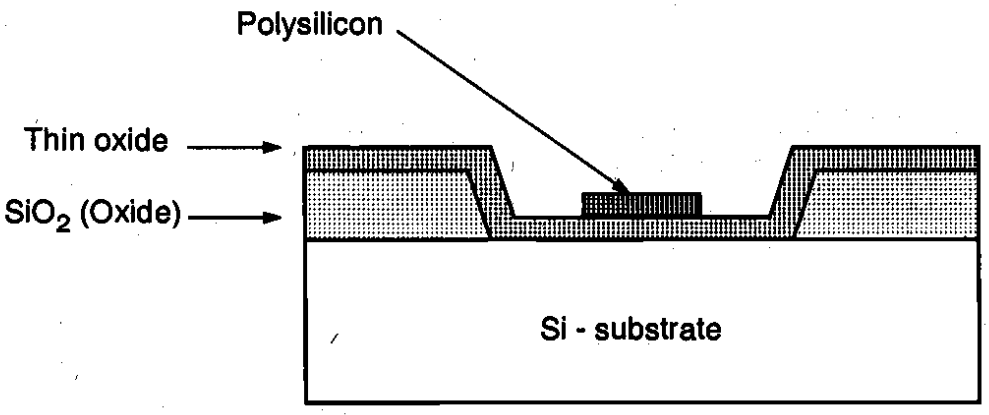
The areas which are not shielded from the UV light by the opaque mask features become insoluble, whereas the shielded areas can subsequently be etched away by a developing solution. Negative photo-resists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photo-resists. Therefore, negative photo-resists are-used less commonly in the manufacturing ofhigh-density integrated circuits.

FabricationtheNmosTransistor

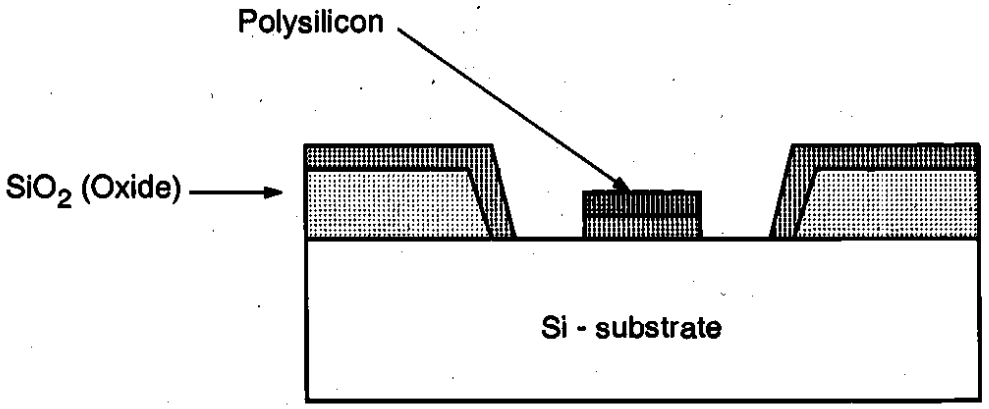
The process starts with of silicon substrate (Fig. (a)), in which a relatively thick dioxide layer, also called field oxide, iscreatedonthe surface (Fig. (b)).Then, the field oxide is selectivelyetched to expose the siliconsurface onwhichthe MOS transistor will be created (Fig. (c)). Following this step, the surface is covered with a thin, high-quality oxide layer, which will eventually form the gate oxide of the n- mos transistor On top of the thin oxide layer, a layer ofpolysilicon(polycrystallinesilicon) isdeposited(Fig. (e)). Polysiliconisused both as gate electrode material for MOS transistors and also as an interconnect medium in silicon integrated circuits. Undoped polysilicon has relatively high resistivity. The-resistivity ofpolysilicon can be reduced, however, bydoping it with impurityatoms.

After deposition, the polysilicon layer is patterned and etched to formthe interconnects and the MOS transistor gates (Fig. (f)). The thin gate oxide not covered by polysilicon is also etched away, which exposes the bare silicon surface on which the source and drainjunctions are to be formed (Fig. (g)). The entire silicon surface is then doped with a high concentration of impurities, either through diffusion or ionimplantation (in this case with donor atoms to produce n-type doping). Figure (h) shows that the doping penetrates the exposed areas on the silicon surface, ultimately creating two ntype regions (source and drain junctions) in the p-type substrate. The impurity doping also penetrates the polysilicon on the surface, reducing its resistivity. Note that the polysilicon gate, which is patterned *before* doping, actually defines the precise location of the channel region and, hence, the location of the source and the drain regions. Since this procedure allows very precise positioning of the two regions relative to the gate, it is also called the *self-alignedprocess.*


Si - substrate
(a)
SiO_2 (Oxide)
Si - substrate
(b)
SiO_2 (Oxide)
Si - substrate
(c)
Thin oxide
SiO_2 (Oxide)
Si - substrate
(d)
Polysilicon
Thin oxide
SiO_2 (Oxide)
Si - substrate
(e)

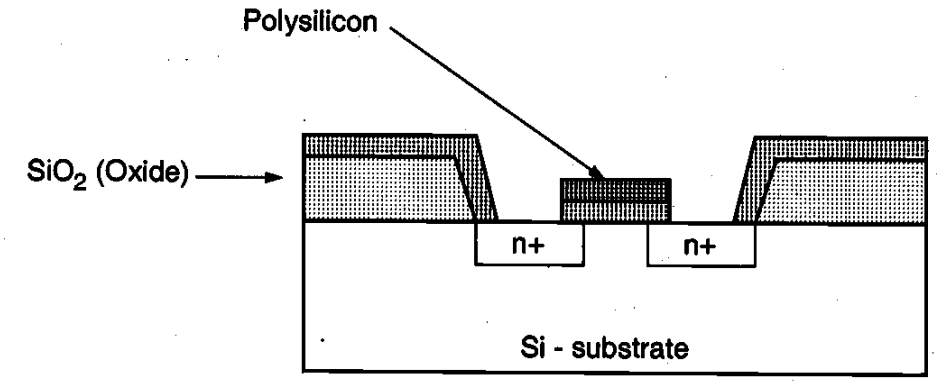


(f)

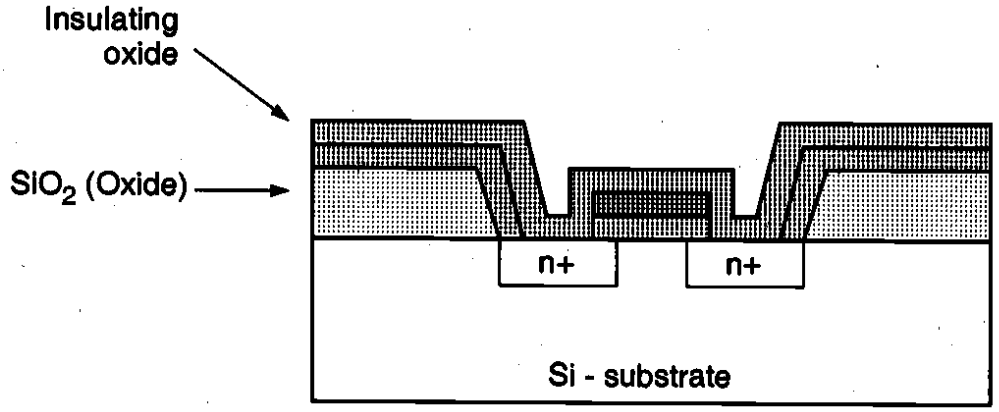


(g)

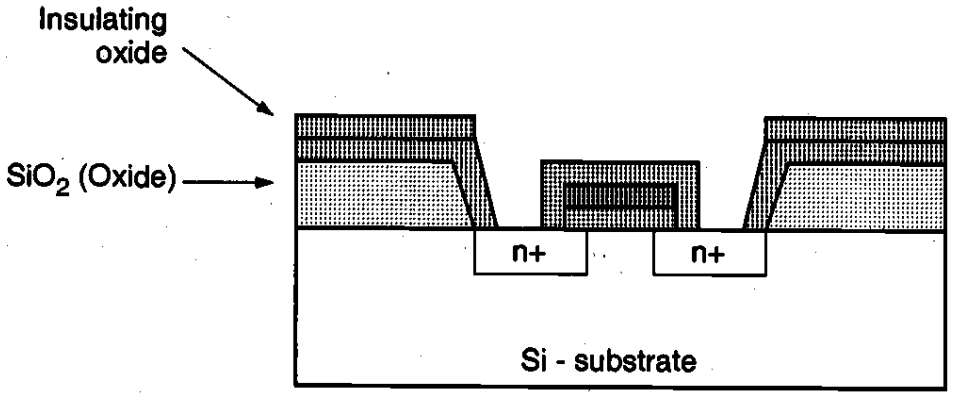
Once the source and drain regions are completed, the entire surface is again covered with an insulating layer of silicon dioxide (Fig. (i)). The insulating oxide layer is then patterned in order to provide contact windows for the drain and source junctions (Fig.(j)). The surface is covered with evaporated aluminum which will form theinterconnects (Fig. (k)). Finally, the metal layer is patterned and etched, completing the interconnection of the MOS transistors on the surface (Fig. (1)). Usually, a second (and third) layer of metallic interconnect can also be added on top of this structure by creating another insulating oxide layer, cutting contact(via) holes, depositing, and patterning the metal. The major process steps for the fabrication of an nMOS transistor on p-type silicon substrate are also illustrated in Plate 1 and Plate 2.


Polysilicon
SiO_2 (Oxide)
n+
n+
Si - substrate

(h)


Insulating oxide
SiO_2 (Oxide)
n+
n+
Si - substrate

(i)


Insulating oxide
SiO_2 (Oxide)
n+
n+
Si - substrate

(j)

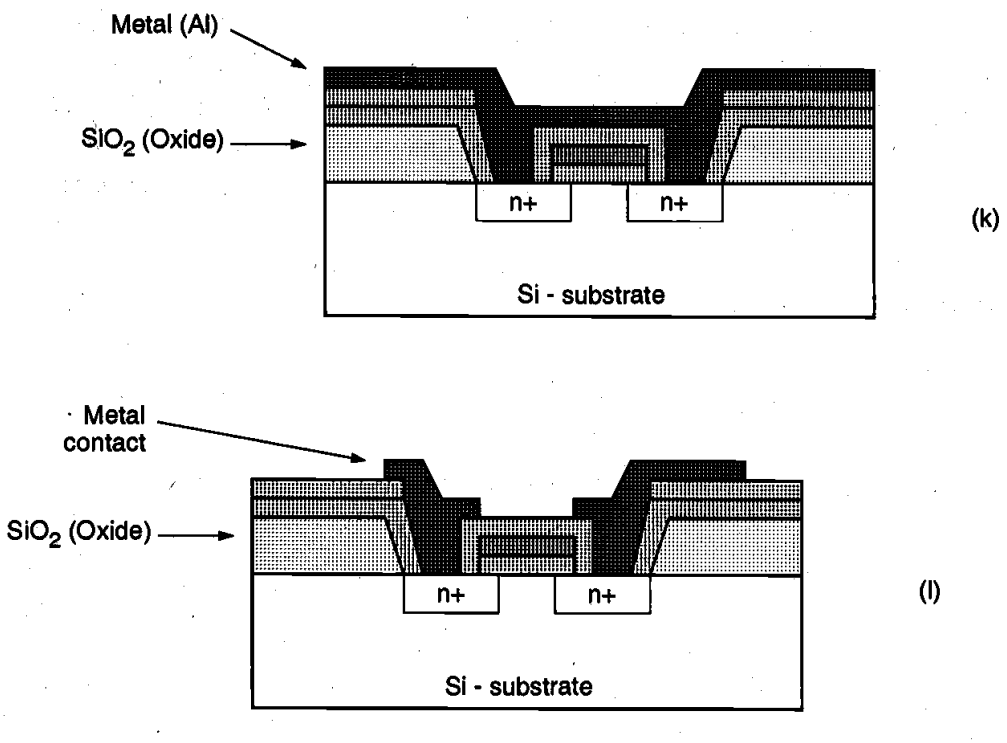
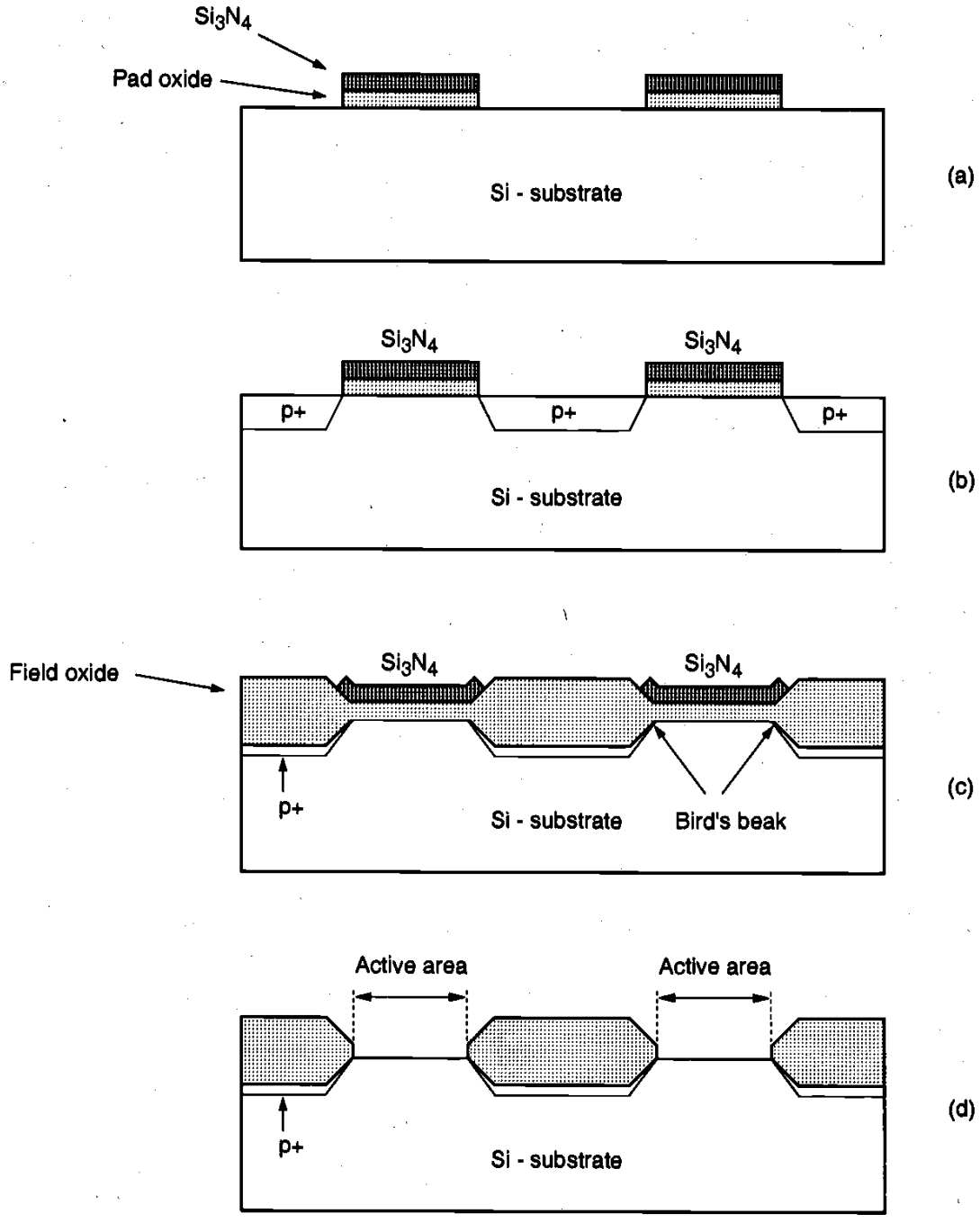


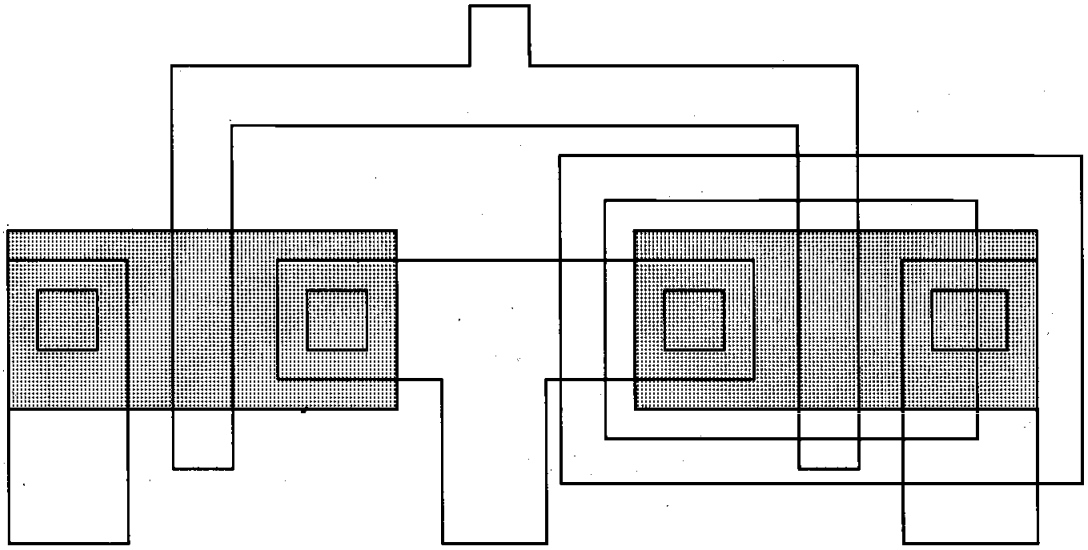
*Figure2.4.*Processflowforthefabricationofann-typeMOStransistor

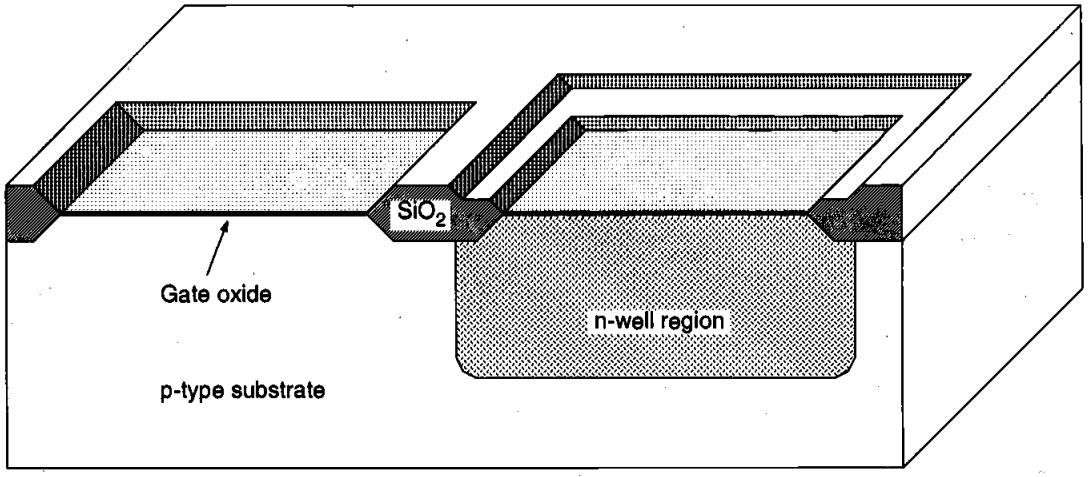
TheCMOSn-WellProcess

Having examined the basic process steps for pattern transfer through lithography and having gone throughthe fabrication procedureofa single n-type MOS transistor, we can now return to the generalized fabrication sequence of n-well CMOSintegrated circuits, as shown in Fig. 1. In the following figures, some of the important process steps involved in the fabrication of a CMOS inverter will be shown by a top view of the lithographic masks and a cross-sectionalview ofthe relevant areas. The n-wellCMOS process starts witha moderately doped (with impurity concentration typically less than 1015 cm-3) p-type silicon substrate. Then, an initialoxide layer isgrownonthe entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this windowin the oxide.

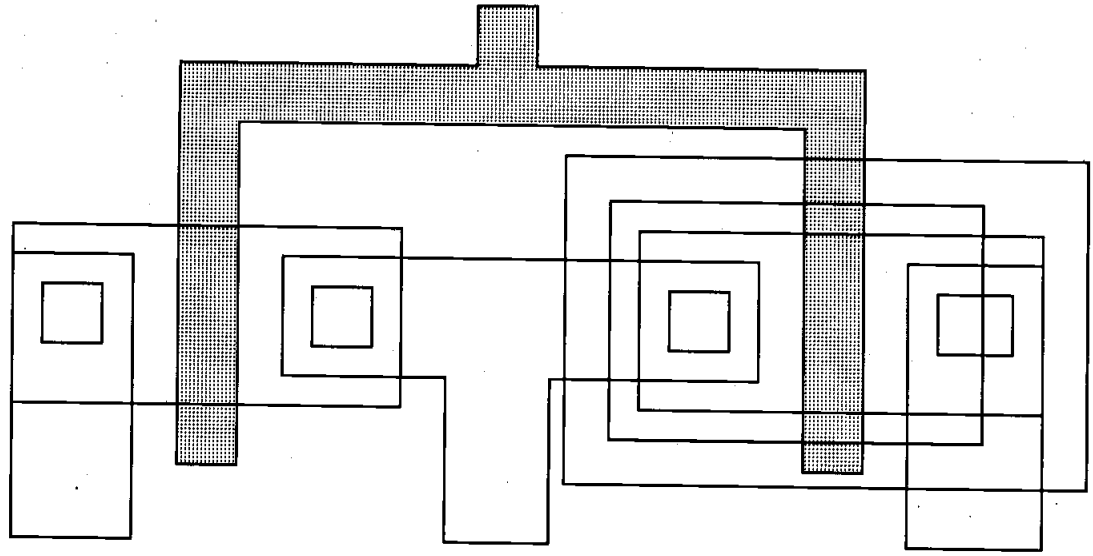
Once the n-wellis created, the active areas ofthenMOS and pMOS transistors canbe defined. Figures 2.6 through 2.11 illustrate the significant milestones that occur during the fabrication process of a CMOS inverter. The main process steps for the fabrication of a CMOS inverter are also illustrated in Plate 3, Plate 4 and Plate 5.

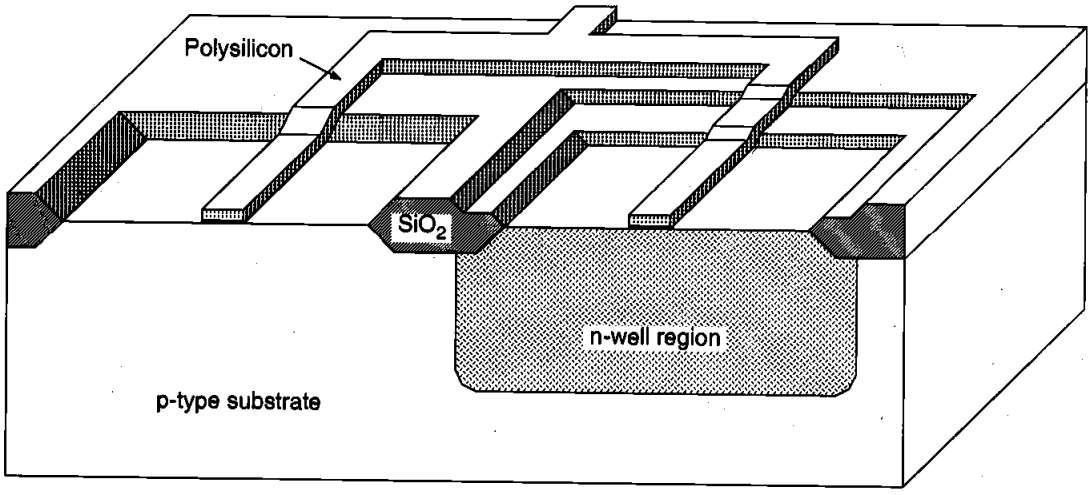

Si_3N_4
Pad oxide
Si - substrate
(a)
Si_3N_4
Si_3N_4
p+
p+
p+
Si - substrate
(b)
Field oxide
Si_3N_4
Si_3N_4
p+
Si - substrate
Bird's beak
(c)
Active area
Active area
p+
Si - substrate
(d)



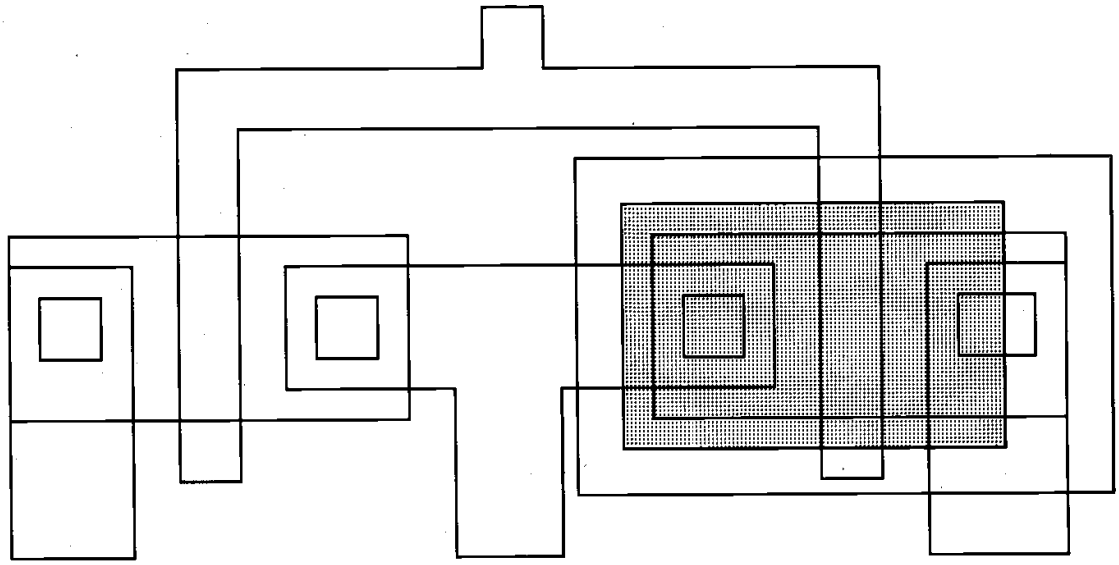


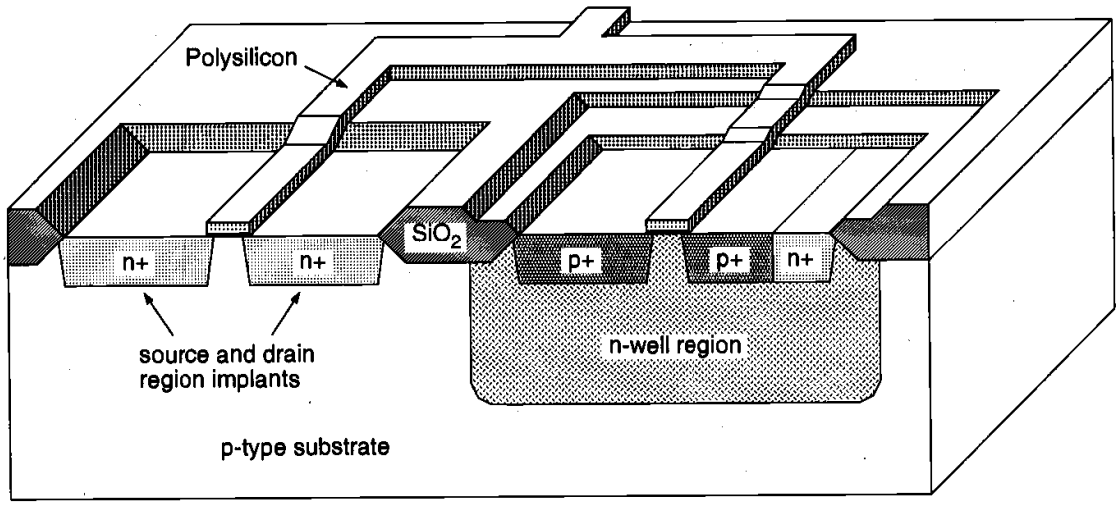
Following the creation of the n-well region, a thick field oxide is grown in the areas surrounding the transistor's active regions, and a thin gate oxide is grown on topofthe active regions



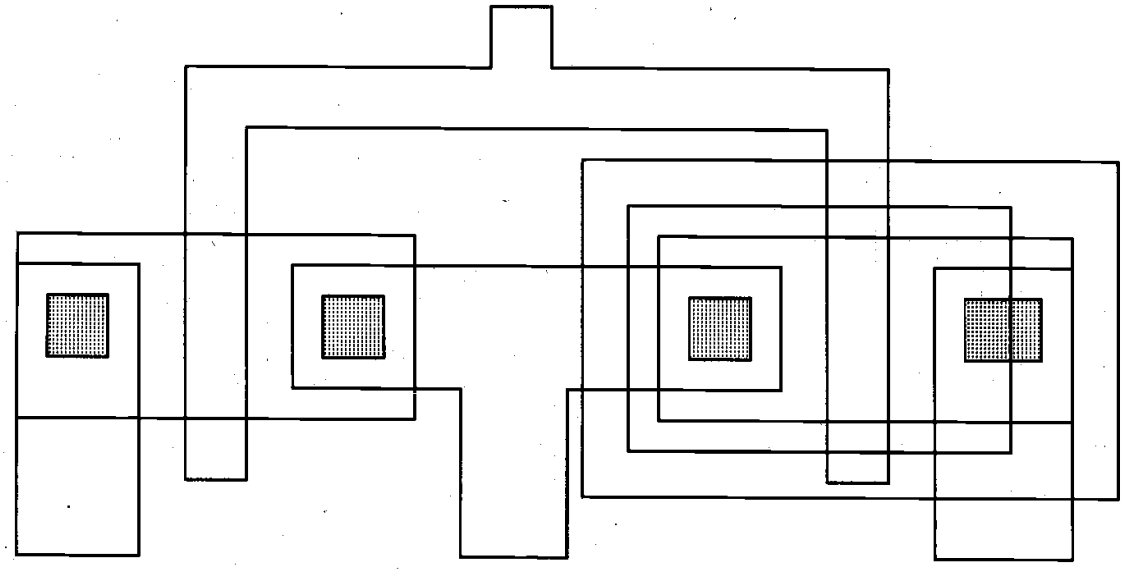


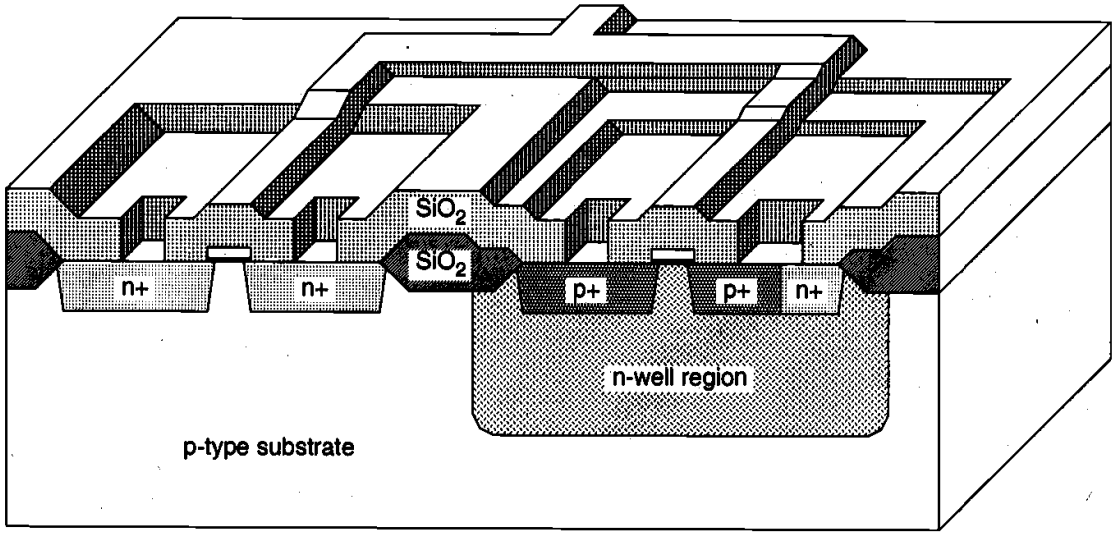
The polysilicon layer is deposited using chemical vapor deposition (CVD) and patterned by dry (plasma) etching. The created polysilicon lines will function as the gate electrodes ofthe nMOS and the pMOS transistors and their interconnects.



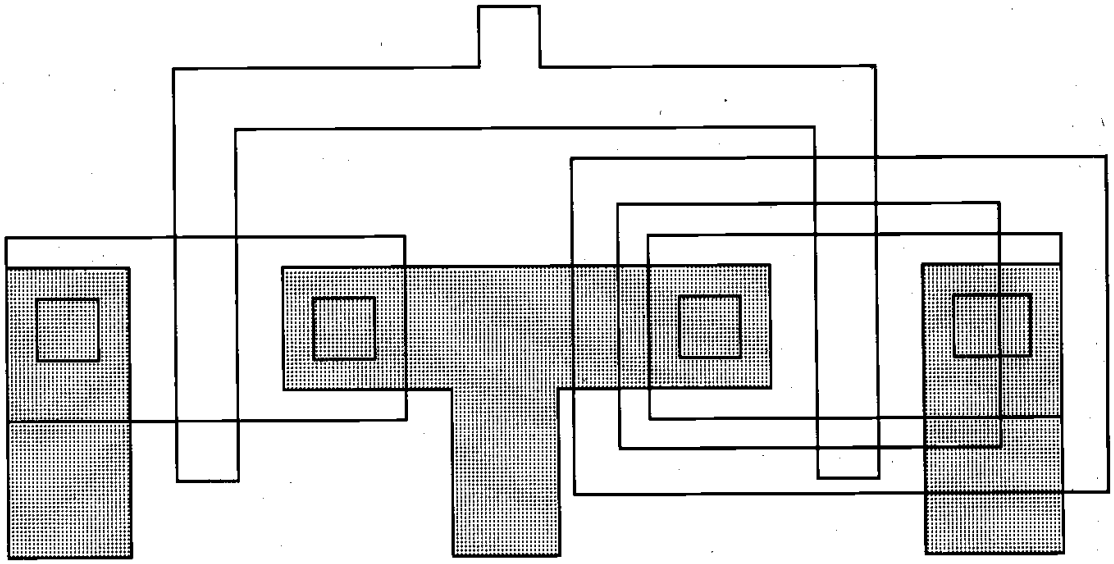


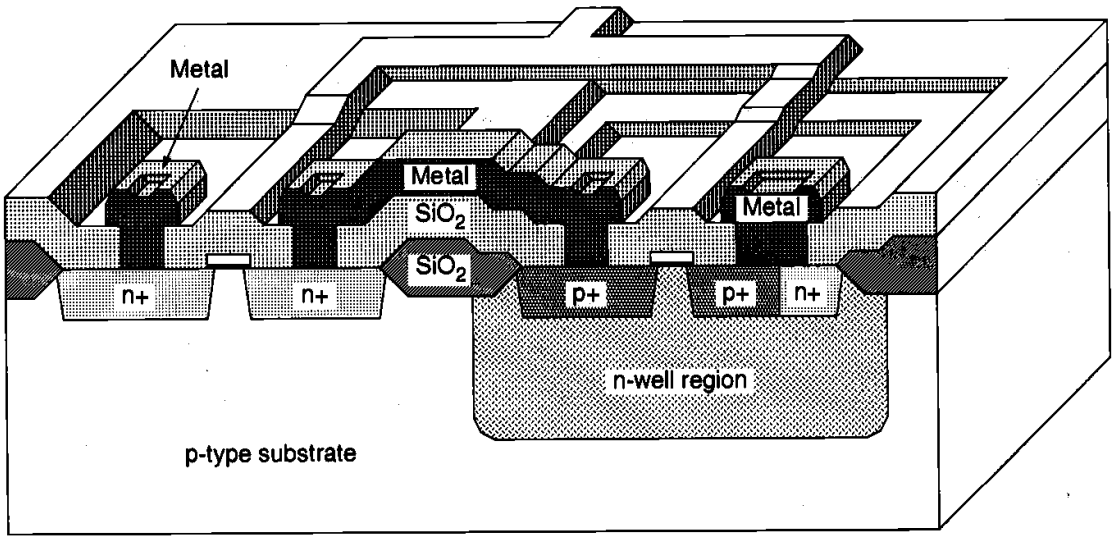
Usingaset oftwomasks,then+andp+regionsare implanted intothesubstrateand into the n-well, respectively.



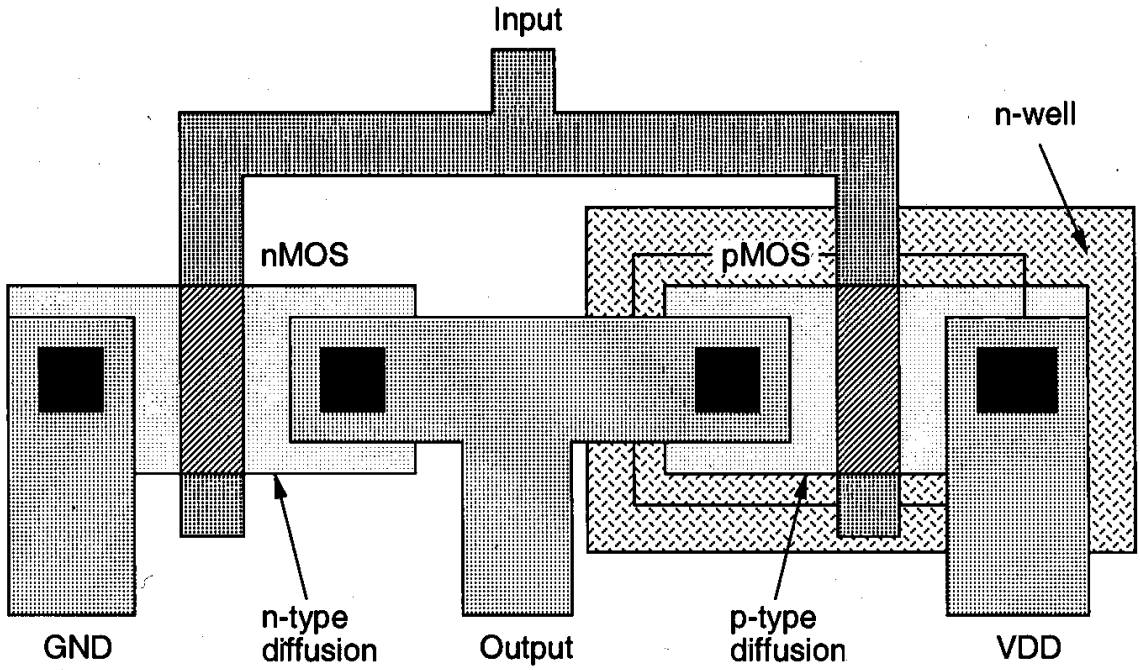


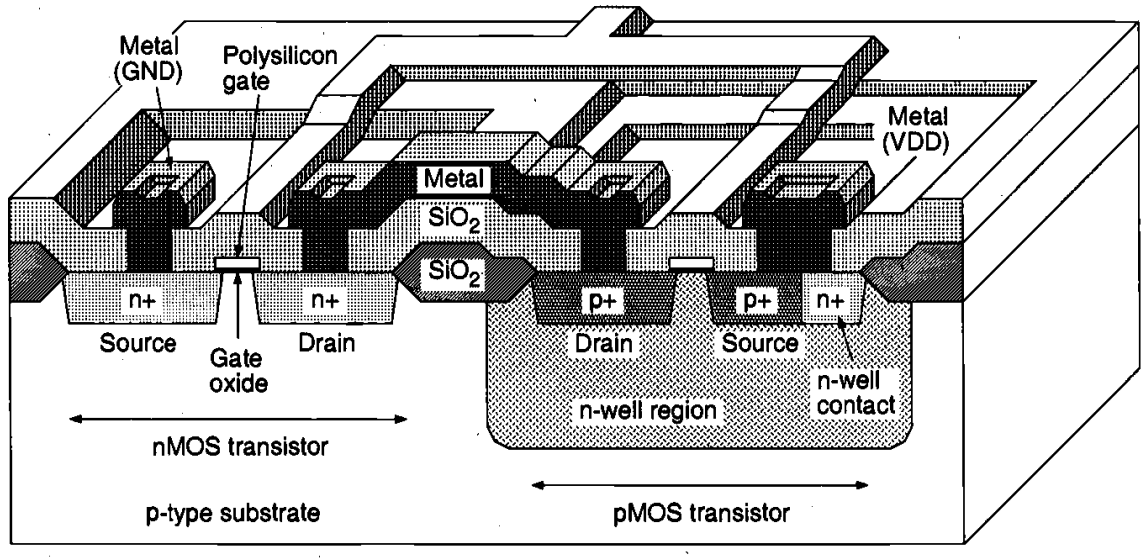
An insulating silicon dioxide layer is deposited over the entire wafer using CVD. Then, the contacts are defined and etched away to expose the silicon or polysilicon contact windows.Thesecontact windowsarenecessarytocompletethecircuit interconnectionsusing the metal layer,





Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.





The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (in the n-well), and the poly-silicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except over wire-bonding pad areas

ExplainDesignrulesLayoutLayoutDesign

Rules

The physical mask layout ofanycircuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features.

Thedesignrulesareusuallydescribedintwoways:

(i) Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of absolute dimensions in micrometers, or,

(ii) Lambda rules, which specify the layout constraints in terms of a single parameter () and thus allow linear, proportional scaling of allgeometrical constraints.

Lambda-based layout design rules were originally devised to simplify the industry standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized,

Activearearules

Minimum active area width 3λ

Minimumactiveareaspacing3λ

Polysilicon rules

Minimum poly width 2 λ

Minimumpolyspacing2λ

Minimumgateextensionofpolyoveractive2λ Minimum

poly-active edge spacing L λ

(polyoutsideactivearea)

Minimumpoly-activeedgespacing3λ

(poly inside active area)

Metalrules

Minimum metal width 3 λ

Minimummetalspacing3λ **Contact**

rules

Polycontactsize2 λ

Minimumpolycontactspacing2λ

STICK DIAGRAM

It is the Stick and colour representation of the n- mos and c-mos circuit presentation and constructed as per the given rules

We havefollow the rules as per the NAND and NOR gate constructions that is series connection in n- mos for NAND and parallel connection in p-mos similarly parallel connection for NOR gate in n-mos and series in p-mos

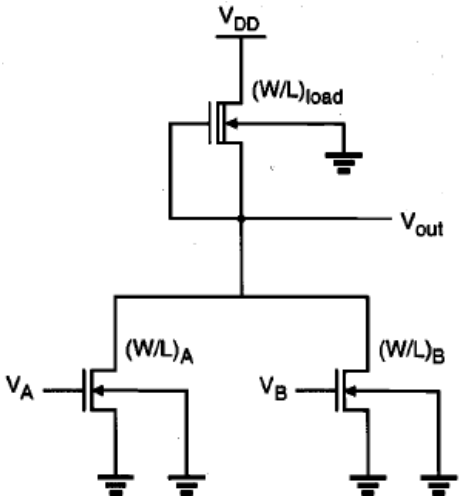


FIG.CIRCUITDIAGRAMOFNORGATE

Example-NORGATE

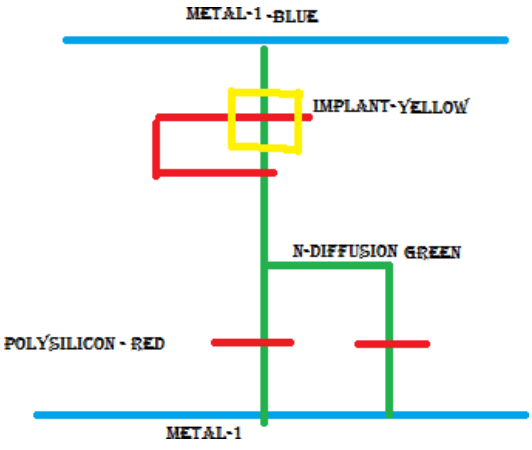


FIG. STICKDIAGRAMOFNORGATE.

Similarlyeveryother gatecanconstructed followingtheseconditions.

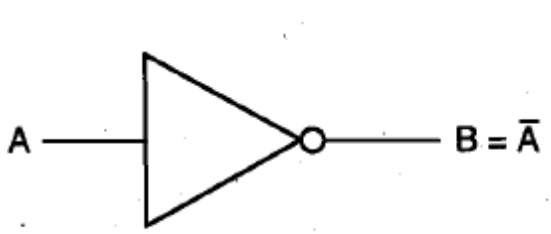
Full-CustomMaskLayoutDesign

In this section, the basic mask layout principles for CMOS inverters and logic gates will be presented. The design of physical layout is very tightly linked to overall circuit performance (area, speed, and power dissipation) since the physical structure directly determines the trans-conductance ofthe transistors, the parasitic capacitances and resistances, and obviously, the silicon area which is used for a certain function. On the other hand, the detailed masklayout of logic gates requires a very intensive and time consuming design effort, which is justifiable only in special circumstances where the area and/or the performance of the circuit must be optimized under very tight constraints. Therefore, automated layout generation (e.g., using a standard cell library, computer aided placement- and-routing) is typically preferred for the design of most digital VLSI circuits. In order to judge the physical constraints and limitations, however, the VLSI designer must also have a good understanding of the physical mask layout process.

UNIT-3
MOSInverter

BasicNMOSinverters, characteristics,

The logic symbol and the truth table of the ideal inverter are shown in Fig. 1. In MOS inverter circuits, boththe input variable A and the output variable B are represented by node voltages, referenced to the ground potential. Using positive logic convention, the Boolean (or logic) value of"1" can be represented by a high voltage ofV_{DD}, and the Boolean (or logic) value of "0" can be represented by a low voltage of 0. The DC voltage transfer characteristic (V_{TC}) of the ideal inverter circuit is shown in Fig. 2. The voltage $V_{th}$is called the inverterthreshold voltage. Notethat for anyinput voltagebetween0and$V_{th}=V_{DD}/2$, the output voltage is equal to V_{DD}(logic" 1).



Symbol

A	B
0	1
1	0

Truth Table

Fig.1,2Logicsymbolandtruthtableoftheinverter

The output switches from V_{DD} to 0 when the input is equal to V_{th}. For any input voltage between V_{th} and V_{DD}, the output voltage assumes a value of 0 (logic "0"). Thus, an input voltage 0 < Vi. < V is interpreted by this ideal inverter as a logic "0," while an input voltage V_{th} <Vin < V_{DD} s interpreted as a logic " 1." The DC characteristics of actual inverter circuits will obviously differ in various degrees fromthe ideal characteristic shown in Fig. 2. The accurate estimation and the manipulation of the shape of V_{TC} for various inverter types are actually important parts of the design process.

Figure 3 shows the generalized circuit structure of an nMOS inverter. The input voltage of the inverter circuit is also the gate-to-source voltage of the nMOS transistor (V_{in} = V_{Gs}), while the output voltage of the circuitis equal to the drain-to-source voltage (V_{out}= V_{DS}). The source and the substrate terminals of the nMOS transistor, also called the driver transistor, are connected to ground potential; hence,

the source-to-substrate voltage is V_{SB} = 0. In this generalized representation, the load device is represented as a two-terminal circuit element with terminal current IL and terminal voltage $V_L(I_L)$.

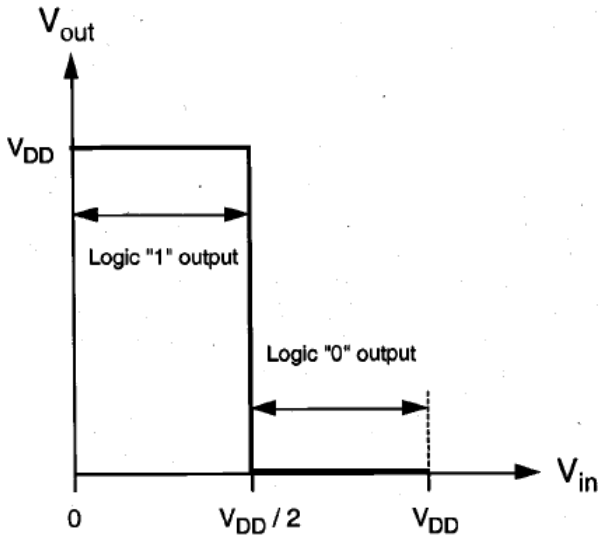


Fig3 Voltagetransfercharacteristic(VTC)oftheidealinverter.

VoltageTransferCharacteristic(VTC*)*

Applying Kirchhoff s Current Law (KCL) to this simple circuit, we see that the load current is always equal to the nMOS drain current.

$$I_D(V_{in}, V_{out}) = I_L(V_L) \quad \text{.....(1)}$$

The voltage transfer characteristic describing ***V*** as a function of Vin under DC conditions can then be found by analytically solving equation (1) for various input voltage values. The typicalVTC ofa realistic nMOS inverter is shown in Fig. Upon examination, we can identify a number of important properties ofthis DC transfer characteristic.

The general shape of the VTC in Fig. 5.4 is qualitatively similar to that of the ideal inverter transfer characteristic shown in Fig. 5.2. There are, however, several significant differences that deserve special attention. For very low input voltage levels, theoutput voltage V is equal to the high value of *VOH (output high voltage)*. In this case, the driver nMOS transistor is in cut-off, and hence, does not conduct any current. Consequently, the voltage dropacrossthe load device isverysmall in magnitude, and theoutput voltage level is high. As the input voltage V increases, the driver transistor starts conducting a certain drain current,andtheoutputvoltageeventuallystartstodecrease.Noticethatthisdropinthe

outputvoltage leveldoesnotoccurabruptly, suchastheverticaldropassumed fortheideal inverter VTC, but rather gradually and with a finite slope.

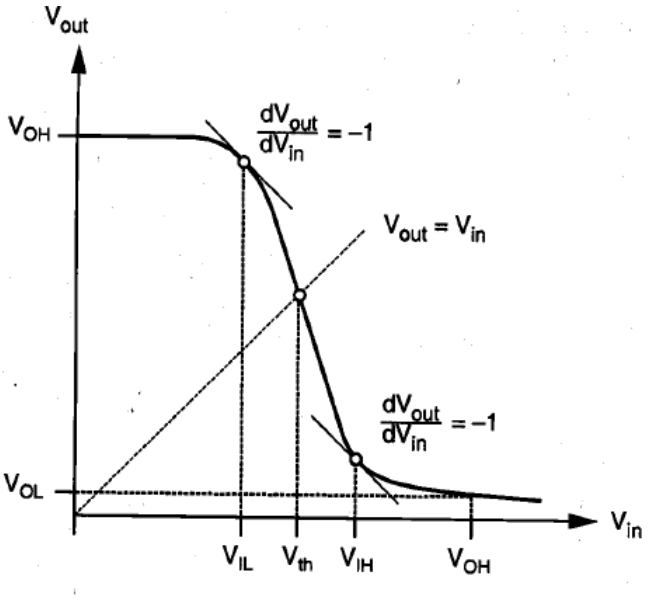


*Figure**5.4.***TypicalvoltagetransfercharacteristicofarealisticnMOSinverter.

We identifytwo *criticalvoltagepoints*onthiscurve, wheretheslopeofthe Vt(Vin) characteristic becomes equal to -1, i.e.,

$$\frac{dV_{out}}{dV_{in}} = -1$$

VOH: Maximumoutput voltage whenthe output level is logic " 1"

VOL Minimum output voltage when the output level is logic "0"

VIL:Maximuminput voltagewhichcanbe interpretedaslogic"0"

VIH:Minimuminputvoltagewhichcanbeinterpretedaslogicⁿ1"

Describeinverterswithresistiveloadandwithn-type&MOSFETloadResistive- Load Inverter

The basic structure of the resistive-load inverter circuit is shown in Fig. 1. As in the general inverter circuit as shown in Fig. 2, an enhancement-type nMOS transistor acts as the driver device. The load consists of a simple linear resistor, RL. The power supply voltage of this circuit is VDD. Since the following analysis concentrates on the static behavior of the circuit, the output load capacitance is not shown in this figure.

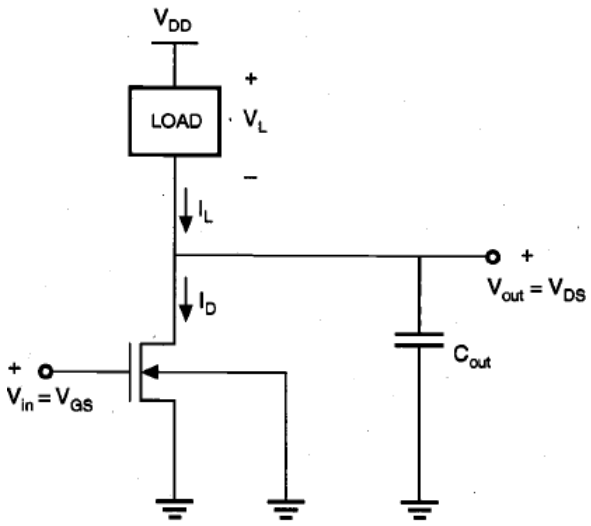


Fig.1

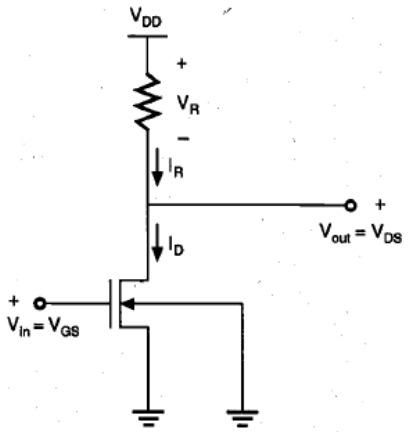


Fig.2

As already noted in Section equation 1, the drain current IDof the driver MOSFET is equal to the load current R in DC steady-state operation. To simplify the calculations, the channel-length modulation effect will be neglected in thefollowing, i.e., A = 0. Also, note that the source andthe substrate terminals of the driver transistor are both connected to the ground; hence, VSB = 0. Consequently, the threshold voltage of the driver transistorisalways equal to V.. We start our analysis by identifying the various operating regions of the driver transistor under steady-state conditions. For input voltages smaller than the threshold voltage V., the transistor is in cut-off, and does not conduct any drain current. Since the voltage drop across the load resistor is equal to zero, the output voltage must be equal to the power supply voltage, VDD. As the input voltage is increased beyond V_{th}., the driver transistor starts conducting a nonzero drain current. Note that the driver MOSFET is initially in saturation,

$$I_R = \frac{k_n}{2} \cdot (V_{in} - V_{T0})^2$$

since its drain-tosource voltage. (VDs= V_{out}) is larger than(V_{in} – V_{GS}.).Thus,

Inverterswith n-TypeMOSFET Load

The simple resistive-load inverter circuit examined in the previous section is not a suitable candidate for most digital VLSI system applications, primarily because of the large area occupied by the load resistor. In this section, we will introduce inverter circuits, which use an nMOS transistor as the *active load* device, instead ofthe linear load resistor.The main advantage ofusing a MOSFET as the load device is that the siliconarea occupied bythe

transistor is usually smaller than that occupied by a comparable resistive load. Moreover, inverter circuits with active loads can be designed to have better overall performance compared to that of passive-load inverters. In a chronological view, the development of inverters with an enhancement-type MOSFET load precedes other active-load inverter types, since its fabrication process was perfected earlier

Enhancement-LoadnMOSInverter

The circuit configurations of two inverters with enhancement-type load devices are shown in Fig. 3 and 4. Depending on the bias voltage applied to its gate terminal, the load transistor can be operated either in the saturation region or in the linear region. Bothtypes of inverters have some distinct advantages and disadvantages from the circuit design point of view.

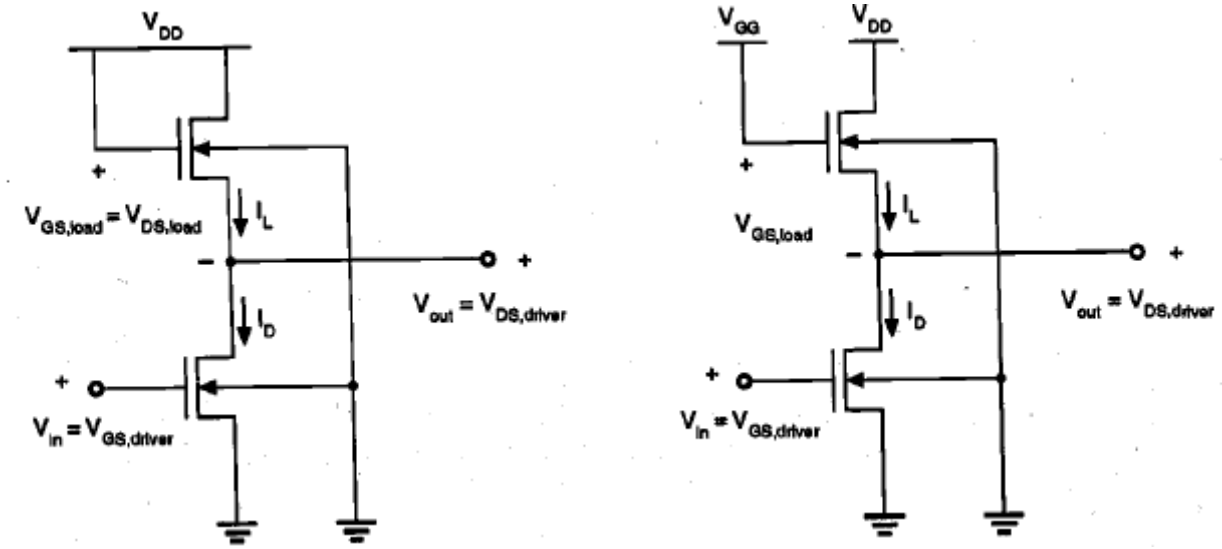


Fig3and4

Depletion-LoadnMOS Inverter

Severalofthe disadvantages ofthe enhancement-type load inverter canbe avoided by using a depletion type nMOS transistor as the load device.-The fabrication process for producing an inverter with an enhancement-type nMOS driver and a depletion-type nMOS load is slightly more complicated and requires additional processing steps, especially for the channel implant to adjust the threshold voltage of the load device.

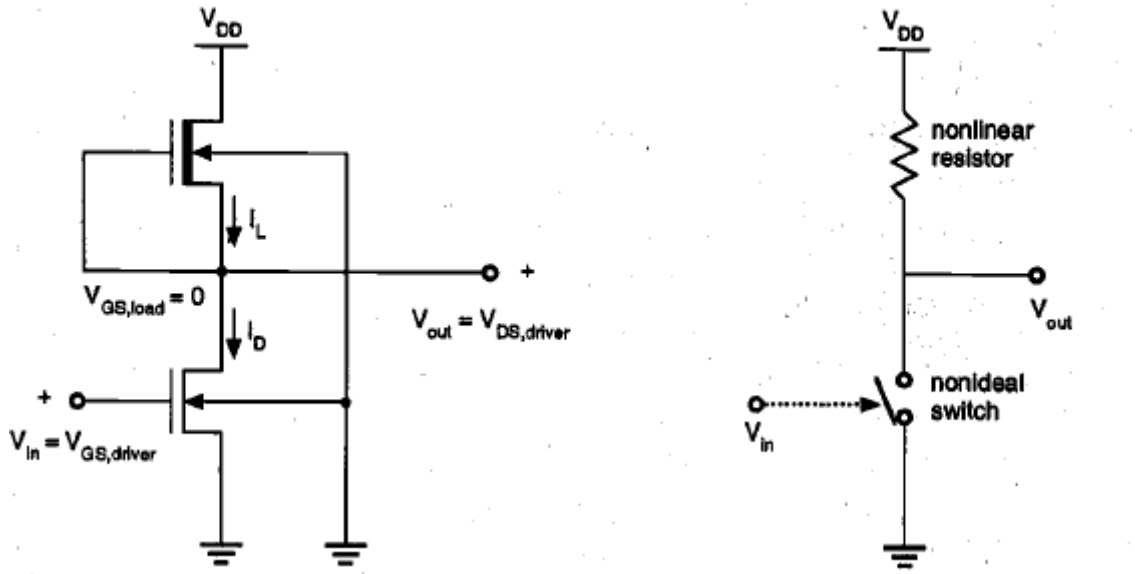


Fig5and6

CMOSinverterandcharacteristicsandinterconnecteffects:Delaytimedefinitions

C – mos which consists of an enhancement-type nMOS transistor and an enhancement-type pMOS transistor, operating in complementary mode (Fig.7 and 8). This configuration is called Complementary MOS (CMOS). The circuit topology is complementary push-pull in the sense that for high input, the nMOS transistor drives (pulls down) the output node while the pMOS transistor acts as the load, and for low input the pMOS transistor drives (pulls up) the output nodewhile the nMOS transistor acts asthe load. Consequently, both devices contribute equally to the circuit operationcharacteristics

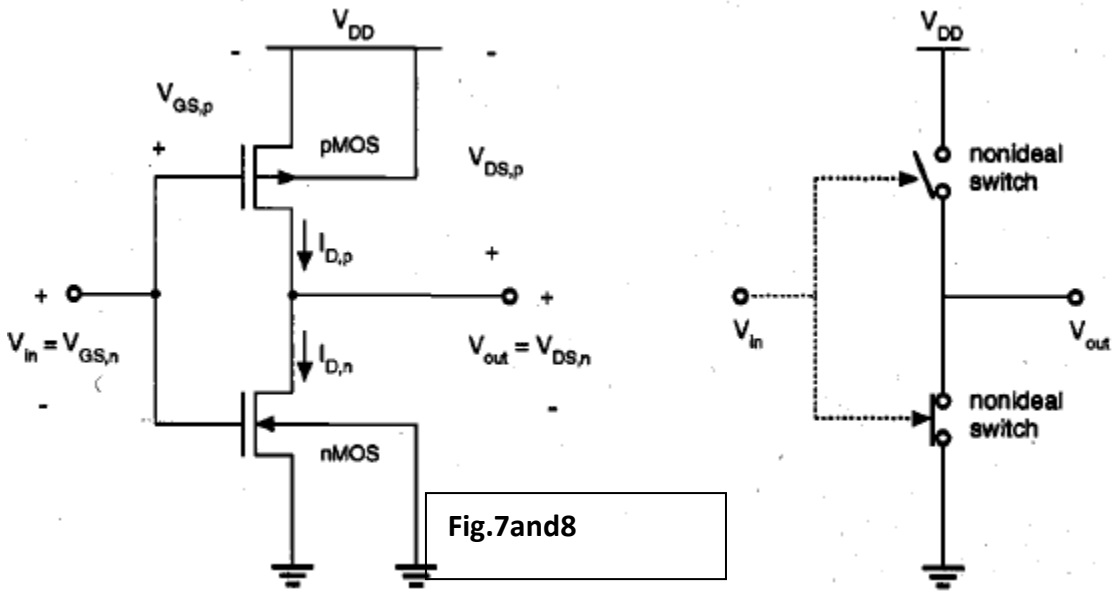


Fig.7and8

(7)CMOSinvertercircuit. (8)Simplified viewoftheCMOS inverter,consistingof two complementary nonideal switches.

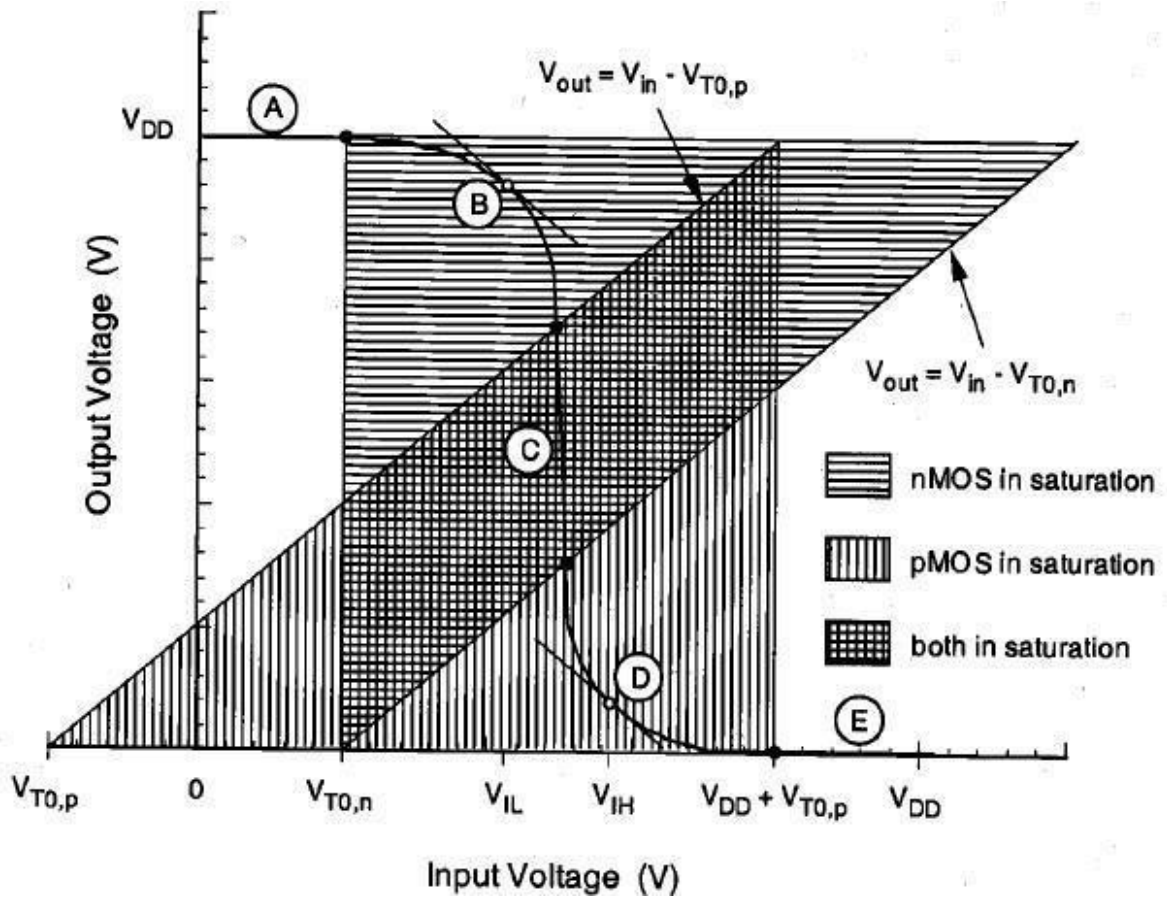


Fig-9 **OperatingregionsofthenMOS andthepMOStransistors.**

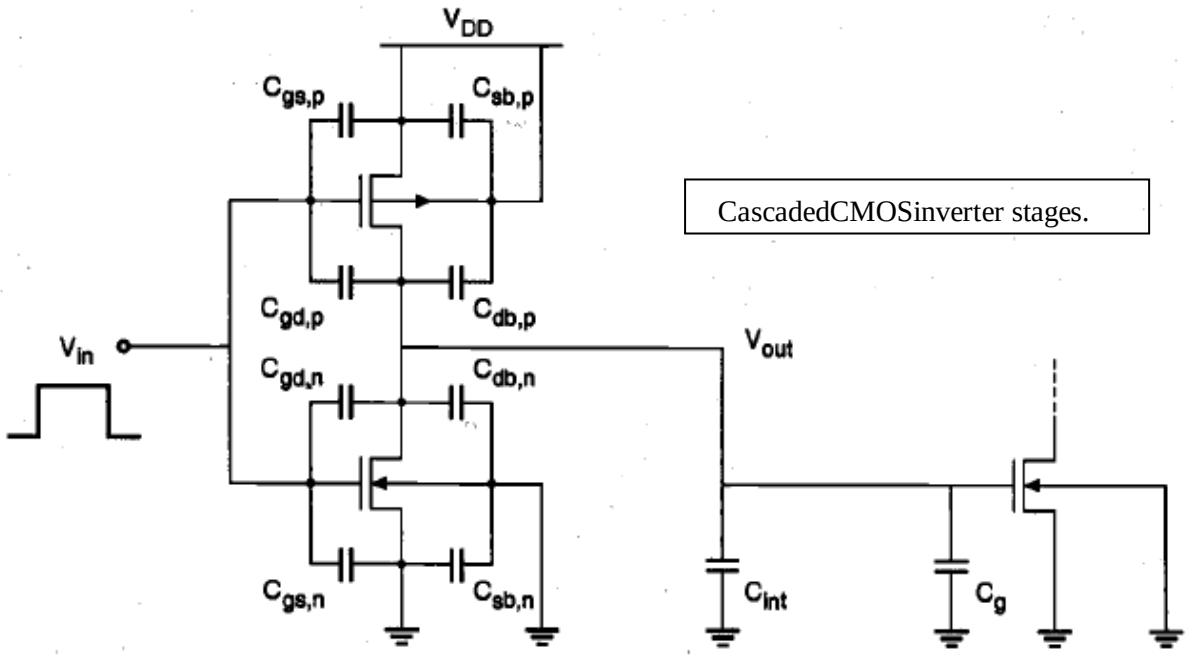
Both of these conditions for device saturation are illustrated graphically as shaded areas on the Vu -V plane in Fig. 9 A typical CMOS inverter voltage transfer characteristic is also superimposed for easy reference. Here, we identify five distinct regions, labeled A throughE,eachcorresponding to a different setofoperating conditions. Thetable below lists these regions and the corresponding critical input and output voltage levels.

Region	V_{in}	V_{out}	nMOS	pMOS
A	$< V_{T0,n}$	V_{OH}	cut-off	linear
B	V_{IL}	high $\approx V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation
D	V_{IH}	low $\approx V_{OL}$	linear	saturation
E	$>(V_{DD} + V_{T0,p})$	V_{OL}	linear	cut-off

Consider the cascade connection of two CMOS inverter circuits shown in Fig. 6.1. The parasitic capacitances associated with each MOSFET are illustrated individually. Here, the capacitances C_{gd} and C_{gs} are primarily due to gate overlap with diffusion, while C_{db} and C_{sb} are voltage-dependent junctioncapacitances, as discussed inChapter 3.The'capacitance component C_g is due to the thin-oxide capacitance over the gate area. In addition, we also considerthelumpedinterconnect capacitanceC_{int},whichrepresentstheparasiticcapacitance contribution ofthe metalor polysilicon connection between the two inverters. It is assumed that a pulse waveform is applied to the input ofthe first-stage inverter.

The problemofanalyzing the output voltage waveformis fairlycomplicated, even for this relatively simple circuit, because a number of nonlinear, voltage-dependent capacitances are involved. To simplifythe problem, we first combine the capacitances seen in Fig. into an equivalent *lumped* linear capacitance, connected between the output node of the inverter and the ground. This combined capacitance at the output node willbe called the load capacitance, $\mathbf{C}_{load}$

$$C_{load} = C_{gd,n} + C_{gd,p} + C_{db,n} + C_{db,p} + C_{int} + C_g$$



CascadedCMOSinverter stages.

Fig -10

The propagation delay times τ_{PHL} and τ_{PLH} determine the input-to-output signal delay during the high to-low and low-to-high transitions of the output, respectively. By definition, $\tau_{PHL}$is the time delay betweenthe V50%-transitionofthe *rising* input voltage and the V50 -

transition of *the falling* output voltage. Similarly, τ_{PLH} is defined as the time delay between the V50 -transition of *the falling* input voltage and the V50%-transition of the *rising* output voltage.

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH})$$

Thus, the propagation delay times τ_{PHL} and τ_{PLH} are found from Fig. 11 as

$$\tau_{PHL} = t_1 - t_0$$

$$\tau_{PLH} = t_3 - t_2$$

The average propagation delay τ_P of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2}$$

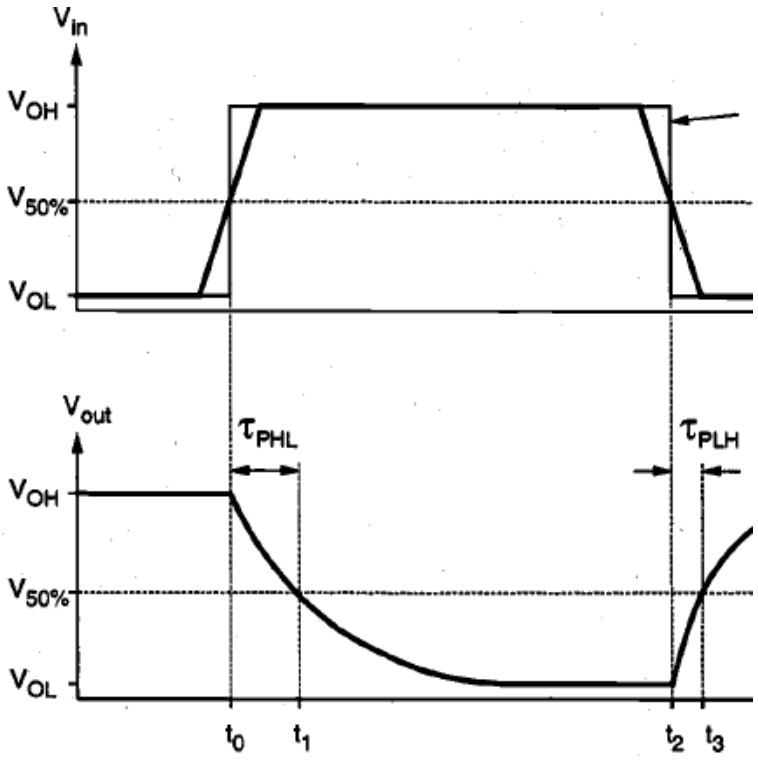


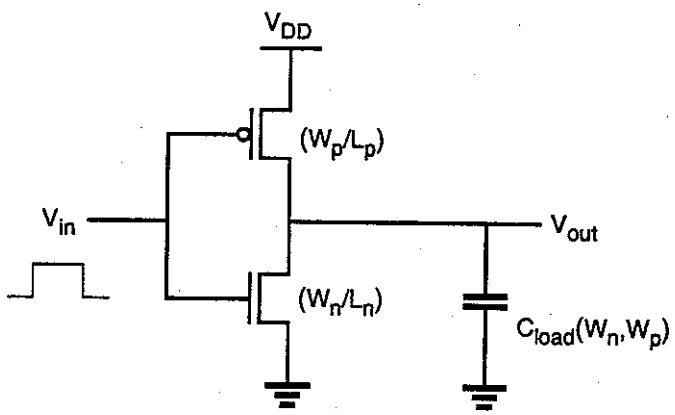
FIG 11(Input and output voltage waveforms of a typical inverter, and the definitions of propagation delay times. The input voltage waveform is idealized as a step pulse for simplicity.)

Invertordesignwithdelayconstraints.

The propagation delayequations on chart 4-5 can be rearranged to solve for W/L, asshownbelow, where wesubstituted $C_{ox}\mu_n(W_n/L_n)$ for k_n and similarlyfor k_pThese

equations canthenbe used to —size‖ a CMOS circuit to achieve a desired minimumrising or falling propagation delay assuming $C_{load}$and other parameters are known

After determining the desired W/L values, we can obtain the device widths W based on the technology minimum design device lengths L . Other constraints such as rise time/falltime or rise/fallsymmetrymayalso need to be considered inadditionto rise and fall delay.



$$\left(\frac{W_n}{L_n}\right)=\frac{C_{load}}{\tau^*_{PHL}\,\mu_n\,C_{ox}\left(V_{DD}-V_{T,n}\right)}\left[\frac{2\,V_{T,n}}{V_{DD}-V_{T,n}}+\ln\left(\frac{4\left(V_{DD}-V_{T,n}\right)}{V_{DD}}-1\right)\right]$$

$$\left(\frac{W_p}{L_p}\right)=\frac{C_{load}}{\tau^*_{PLH}\,\mu_p\,C_{ox}\left(V_{DD}-\left|V_{T,p}\right|\right)}\left[\frac{2\left|V_{T,p}\right|}{V_{DD}-\left|V_{T,p}\right|}+\ln\left(\frac{4\left(V_{DD}-\left|V_{T,p}\right|\right)}{V_{DD}}-1\right)\right]$$

Estimationofparasiticsswitching powerdissipationofCMOSinverters.

equals the instantaneous draincurrent ofthe pMOStransistor. Whenthe input voltage switches from low to high, the Pmos transistor in the circuit is turned off, and the nMOS transistor starts conducting. During this phase, the output load capacitance C_L is being discharged through the nMOS transistor. Thus, the capacitor current equals the instantaneous drain current of the nMOS transistor. When the input voltage switches from high to low, the nMOS transistor in the circuitis turned off, and the pMOS transistor starts conducting. During this phase, the output load capacitance C_L ,ad is being charged up through the pMOS transistor; therefore, the capacitor current

- For complementary CMOS circuits where no dc current flows, average dynamic power is given by

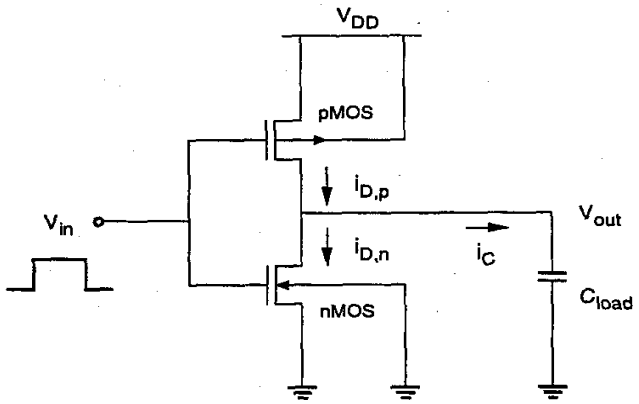
$$P_{ave}=C_L V_{DD}^2 f$$

whereCLrepresentsthetotalloadcapacitance,VDD isthepowersupply,and f is the frequency of the signal transition

– aboveformulaappliesto asimpleCMOS inverterorto complex, combinational CMOS logic

– appliesonlytodynamic(capacitive) power

– dcpowerand/orshort-circuitpowermustbecomputedseparately



UNIT-4

StaticCombinational,Sequential&Dynamicslogic circuits & Memories

MOS logic circuits & CMOSlogic circuits. statestyle, complex logic circuits, pass transistor logic.

In its most general form, a combinational logic circuit, or gate, performing a Boolean function can be represented as a multiple-input single-output system, as depicted in Fig. 6.1. All inputvariables are represented by node voltages, referenced to the ground potential. Using *positive logic convention,* the Boolean (or logic) value of " 1 " can be represented bya high voltage of *VDD,* and the Boolean (or logic) value of "0" can be represented by a low voltage of 0. The output node is loaded with a capacitance *CL,* which representsthecombined parasitic device capacitances in the circuit and the interconnect capacitance components *seen* by the output node. This output load capacitance certainly plays a very significant role in the dynamic operation ofthe logic gate.

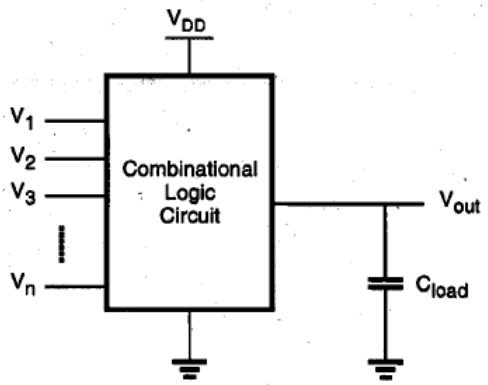
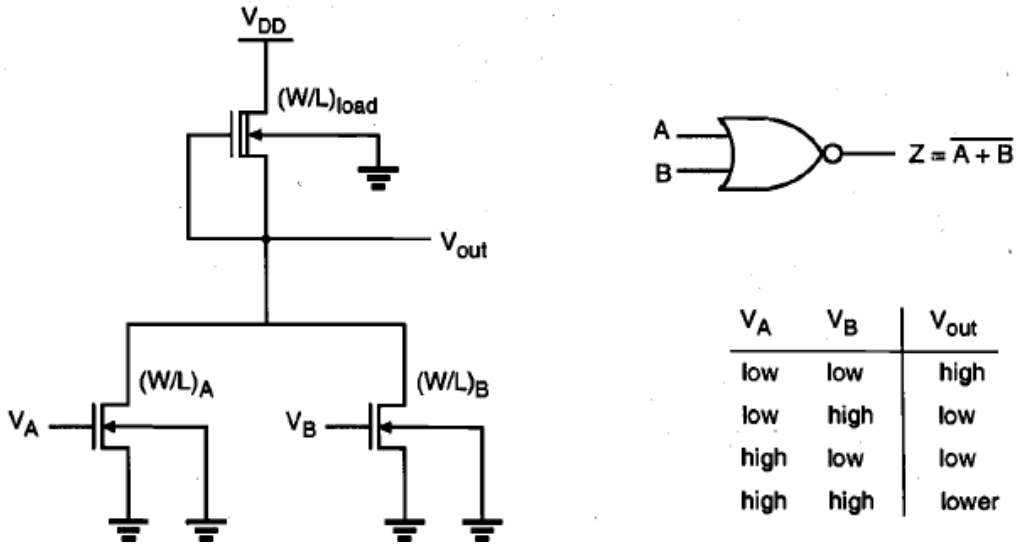


Fig.6.1.

MOSLogicCircuitswithDepletionnMOSLoadsTwo- Input NOR Gate

The first circuit to be examined in this section is the two-input NOR gate. The circuit diagram, the logic symbol, and the corresponding truthtable ofthe gate are given in Fig. 6.2. The Boolean OR operation is performed by the parallel connection of the two enhancement-type nMOS driver transistors.

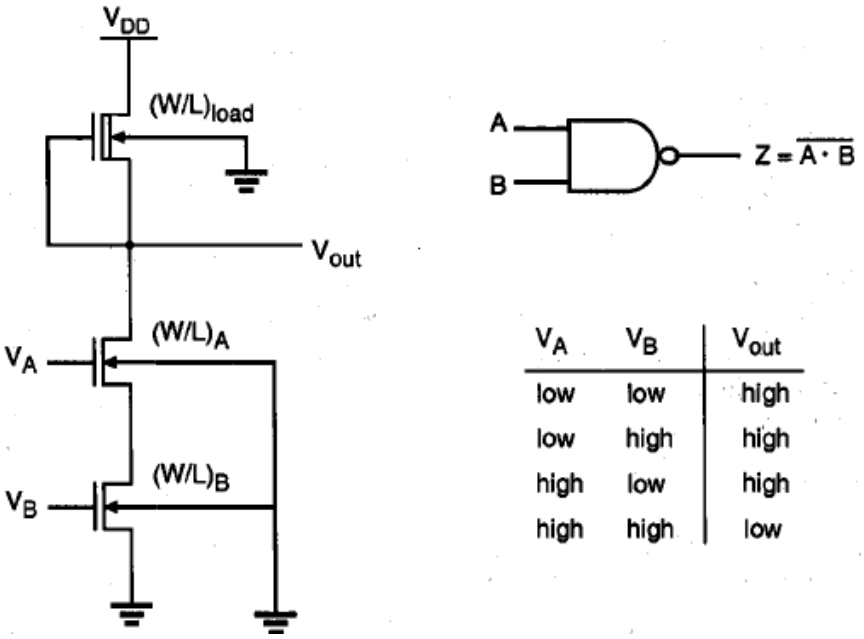


V_A	V_B	V_{out}
low	low	high
low	high	low
high	low	low
high	high	lower

Fig. 6.2.

Two-InputNAND Gate

Next, we will examine the two-input NAND (NAND2) gate. The circuit diagram, the logic symbol, and the corresponding truthtable of the gate are given in Fig. 6.3 The Boolean AND operation is performed by the series connection of the two enhancement type nMOS driver transistors. There is a conducting path between the output node and the ground only if the input voltage V_A *and* the input voltage V_B are equalto logic-high, i.e., only if both of the series-connected drivers are turned on. In this case, the output voltage will below, which is the complemented result of the AND operation. Otherwise, either one or both of the driver transistors will be off, and the output voltage will be pulled to a logic-high level by the depletion-type nMOS load transistor.



V_A	V_B	V_{out}
low	low	high
low	high	high
high	low	high
high	high	low

Fig.6.3

CMOSLogicCircuits

CMOSNOR2(Two-InputNOR)Gate

The design and analysis of CMOS combinational logic circuits can be based on the basic principlesdeveloped forthe nMOS depletion-load logic circuits inthe previoussection. Figure 6.4 shows the circuit diagram of a two-input CMOS NOR gate. Note that the circuit consists ofa parallel-connected n-not and a series-connected complementaryp not. The input voltages *VA* and *VB* are applied to the gatesofone nMOS and one Pmos transistor

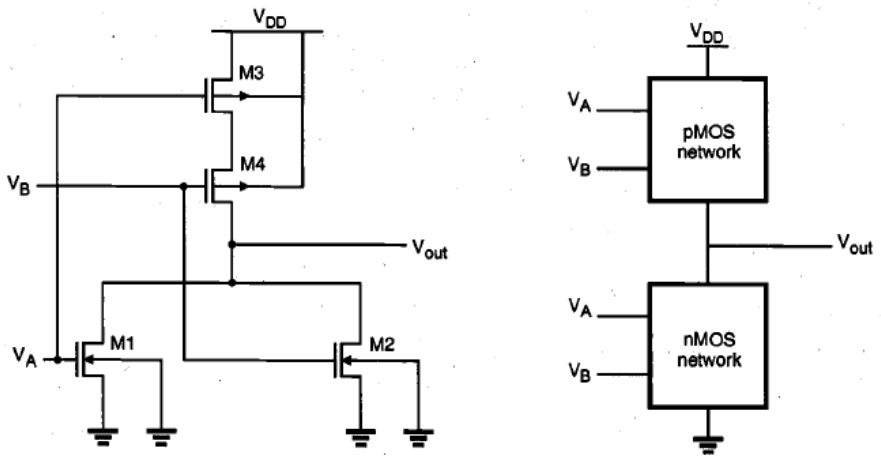


Figure6.4

ComplexLogicCircuits

To realize arbitraryBoolean functions ofmultiple input variables, the basic circuit structuresanddesignprinciplesdeveloped forsimpleNORandNANDgatesinthe

previous sections caneasilybe extended to complex logic gates. The abilityto realize complex logic functions using a small number of transistors is one of the most attractive features of nMOS and CMOS logic circuits.

ConsiderthefollowingBooleanfunctionasanexample.

$$Z = \overline{A(D+E)+BC}$$

The nMOS depletion-load complex logic gate that is used to realize this function is shown in Fig. 6.5 Inspection ofthe circuit topology reveals the simple design principle ofthe pull-down network:

* ORoperationsareperformedbyparallel-connecteddrivers.
* ANDoperationsareperformedbyseries-connecteddrivers.
* Inversionisprovided bythenatureofMOS circuitoperation.

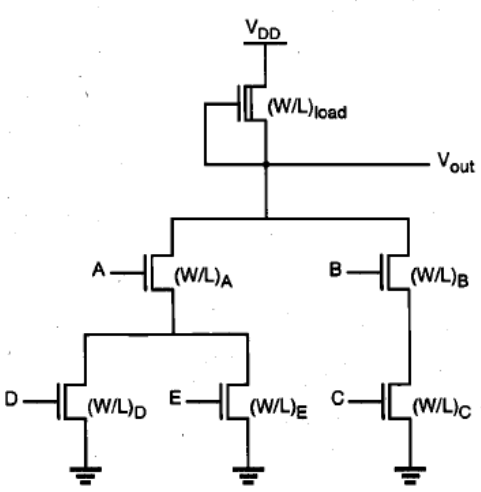


Fig.6.5(nMOScomplexlogicgaterealizingtheBooleanfunction)

The CMOS transmission gate (TG) or pass gate, a new class of logic circuits which use the TGs as their basic building blocks. As shown in Fig 6.6 the CMOS transmission gate consists of one VnMOS and one pMOS transistor, connected in parallel. The gate voltages applied to these two transistors are also set to be complementarysignals. As such, the CMOS TG operates as a bidirectional switch between the nodes A and B which is controlledby signalC.

If the control signal C is logic-high,i.e., equal to*VDD*, then both transistors are turned on and provide a low-resistance current path between the nodes A and B. If, on the other hand, the controlsignal C is low, then both transistors will be off, and the path between thenodes A andB willbe an open circuit.This conditionis alsocalledthehigh-impedance

state. Note that the substrate terminal of the nMOS transistor is connected to ground and the substrate terminal of the pMOS transistor is connected to ***VDD.*** Thus, we must take into account thesubstrate-biaseffect for bothtransistors, depending onthebiasconditions. Figure 7.33 also shows three other commonly used symbolic representations of the CMOS transmission gate.

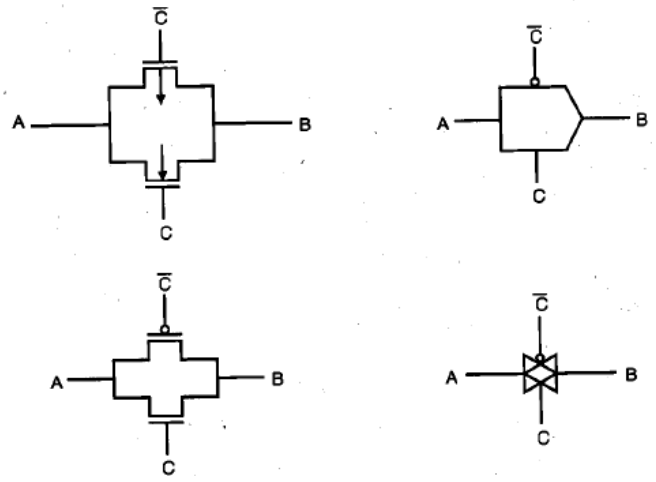


Fig6.6FourdifferentrepresentationsoftheCMOStransmissiongate(TG).

Explain SR latch, clocked latch & flip-flop circuits. TheSR Latch Circuit

The bistable element consisting of two cross-coupled inverters (Fig. 8.2) has two stableoperating modes, orstates.Thecircuit preserves its state(either oneofthetwo possible modes) as long as the power supply voltage is provided; hence, the circuit can perform a simple memory function of *holding* its state. However, the simple two-inverter circuit examined above has no provision for allowing its state to be changed externally from one stable operating mode to the other. To allow such a change of state, we must add simple switches to the bistable element, which can be used to force or trigger the circuit from one operating point to the other. Figure 6.7 shows the circuit structure of the simple CMOS SR latch, which has two such triggeringinputs, S (set) and R (reset). In the literature, the SR latch is also called an SR flip-flop, since two stable states can be switched back andforth.The circuit consists oftwo CMOS NOR2 gates. One ofthe input terminals ofeach NOR gate is used to cross-couple to the output of the other NOR gate, while the second input enables triggering of the circuit.

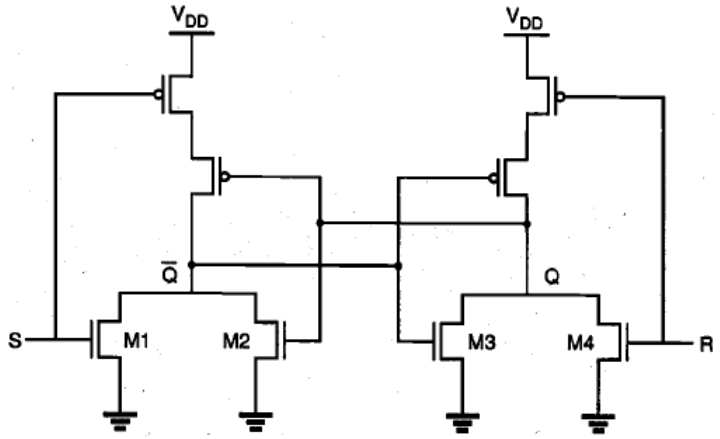


Fig6.7

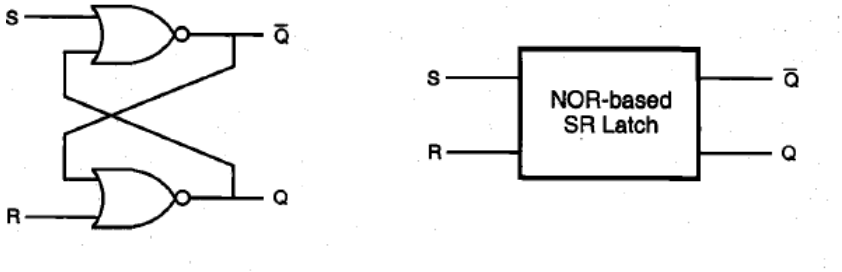


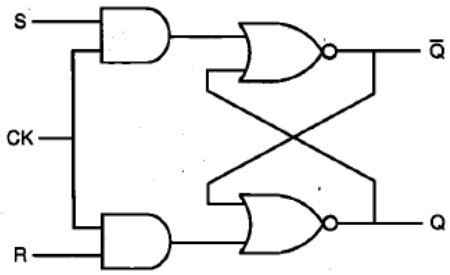
Fig 6.8 (Gate-level schematic and block diagram of the NOR-based SR

latch.)ThetruthtableoftheNOR-basedSRlatchissummarizedinthefollowingtable:

S	R	Q_{n+1}	$\overline{Q_{n+1}}$	Operation
0	0	Q_n	$\overline{Q_n}$	hold
1	0	1	0	set
0	1	0	1	reset
1	1	0	0	not allowed

ClockedSR Latch

All of the SR latch circuits examined in the previous section are essentially asynchronoussequentialcircuits, whichwillrespondtothechangesoccurring ininput signals at a circuit-delay-dependent time point during their operation. To facilitate synchronous operation, the circuit response canbe controlled simplybyadding a gating clock signalto the circuit, so that the outputs will respond to the input levels only during the active period of a clock pulse. For simple reference, the clock pulse will be assumed to be a periodic square waveform, which is applied simultaneouslyto all clocked logic gates inthe system.



6.9(Gate-levelschematicoftheclockedNOR-basedSR latch).

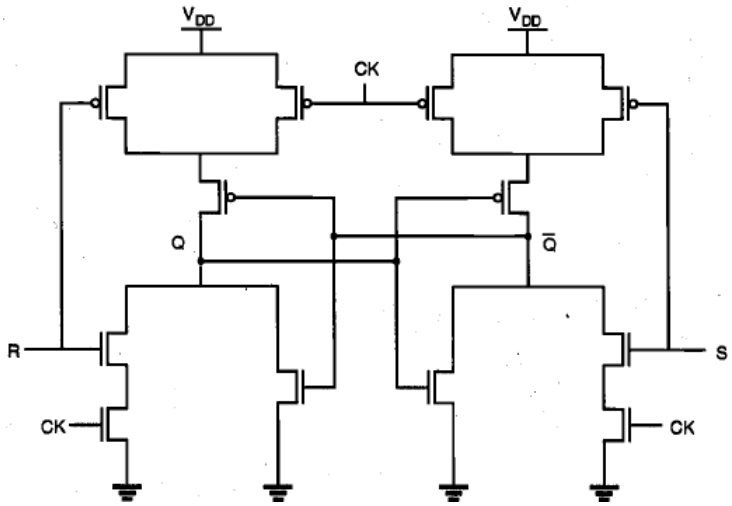


Fig6.10(AOI-basedimplementationoftheclockedNOR-basedSR latchcircuit.)

ExplainDynamiclogic& basicprinciples.

In high-density, high-performance digital implementations where reduction of circuit delay and silicon area is a major objective, *dynamic logic circuits* offer several significant advantages over static logic circuits. The operation of all dynamic logic gates depends on temporary (transient) storage of charge in parasitic node capacitances, instead of relying on steady-state circuit behavior. This operational property necessitates periodic updating of internalnodevoltage levels, sincestoredcharge inacapacitor cannot beretained indefinitely.

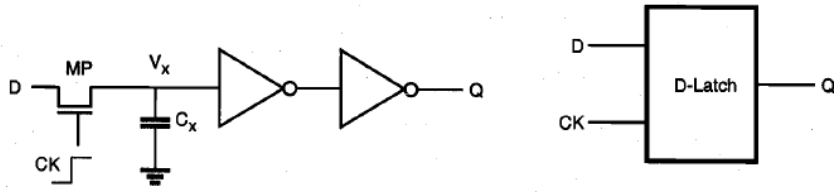


Fig6.11(Dynamiclatchcircuit.)

* When the clock is high (CK = 1), the pass transistor turns on. The capacitor *C,* is either charged up, or charged downthroughthe pass transistor MP, depending on the input (D)voltagelevel. Theoutput (Q)assumesthesamelogiclevelastheinput.

* When the clockislow (CK = 0), the pass transistor MPturns off, and the capacitor C is isolated fromthe input D. Since there is no current path fromthe intermediate node Xto either *VDD* or ground, the amount of charge stored in C. during thepreviouscycle determines the output voltage level Q.

HighperformancedynamicsCMOScircuits.

The circuits presented here are variants of the basic dynamic CMOS logic gate structure.

Theyare designed totake fulladvantageofthe obvious benefits ofdynamic operation and at the same time, to allow unrestricted cascading of multiple stages. The ultimate goal is to achieve reliable, high-speed, compact circuitsusing the least complicated clocking scheme possible.

DominoCMOS Logic

ConsiderthegeneralizedcircuitdiagramofadominoCMOSlogicgateshowninFig. 9.28. A dynamic CMOS logic stage, such as the one shown in Fig. 9.26, is cascaded with a static CMOS inverter stage. The addition of the inverter allows us to operate a numberof such structures in cascade, as explained in the following.

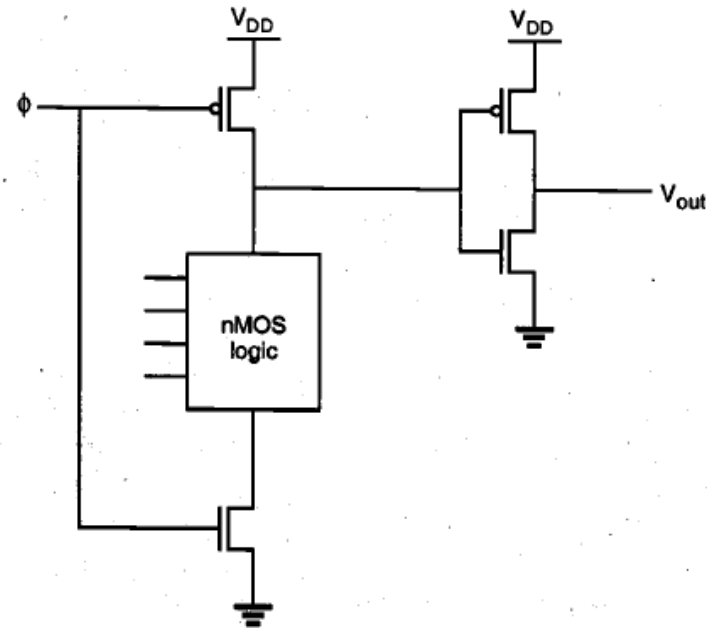


*Figure6.12.*GeneralizedcircuitdiagramofadominoCMOSlogicgate.

During the precharge phase (when CK = 0), the output node of the dynamic CMOS stage is precharged to a high logic level, and the output of the CMOS inverter (buffer) becomes low. When the clock signal rises at the beginning of the evaluation phase, there are two possibilities: The output node of the dynamic CMOS stage is either discharged to a low level through the nMOS circuitry(1 to 0 transition), or it remains high.

Consequently, the inverteroutput voltage can also make at most one transition during the evaluation phase, from 0 to 1. Regardless of the input voltages applied to the dynamic CMOS stage, it is not possible for the buffer output to make a 1 to 0 transition during the evaluation phase.

DefineDynamicRam,SRAM,flashmemory.

Read-write(R/W)memorycircuits,ontheotherhand, must permit themodification (writing) of data bits stored in the memoryarray, as well as their retrieval (reading) on demand. Thisrequiresthatthedatastoragefunctionbe *volatile,* i.e.,thestoreddataarelost when the power supply voltage is turned off. The read-write memory circuit is commonly called *Random Access Memory* (RAM), mostlydue to historical reasons.

Comparedto sequential-accessmemoriessuchasmagnetictapes,anycellintheR/W memoryarraycan be accessed with nearly equal access time. Based on the operation type ofindividualdatastoragecells,RAMsareclassifiedintotwomaincategories: *Static*SRAMs SRAM) and *Dynamic* RAMs (DRAM).

UNIT-5
SystemDesignmethod&Synthesis

Design capture tools, hardware definition languages such as VHDL andpackages. Xlinx (introduction)

Hardwaredescriptionlanguage(HDL):allowsdesignertospecifylogicfunctiononly. Then a computer-aided design (CAD) toolproduces or *synthesizes* the optimized gates. Most commercial designs built using HDLs Two leading HDLs:

– **Verilog**

• developedin1984byGatewayDesignAutomation

• becameanIEEEstandard(1364)in1995

– **VHDL**

VHDL was originally developed at the behest of the U.S Department of Defense in order to document the behavior ofthe ASICs that supplier companies were including in equipment.

The idea ofbeing able to simulate the ASICs fromthe information inthis documentationwas so obviously attractive that logic simulators were developed that could read the VHDL files. The next step wasthe development of logic synthesis tools that readthe VHDL, and output a definition of the physical implementation of the circuit.

The initialversionofVHDL, designedto IEEE standard 1076-1987, includedawiderangeof data types, including numerical (integer and real), logical (bit and boolean), character and time, plus arrays ofbit called bit_vector and ofcharacter called string

Standardization

The IEEE Standard 1076 defines the VHSICHardware Description Language or VHDL. It was originallydeveloped under contract F33615-83-C-1003 fromthe United States Air Force awarded in 1983 to a team with Intermetrics, Inc. as language experts and prime contractor, with Texas Instruments as chip design experts and IBM as computer system design experts. The language has undergone numerous revisions and has a variety ofsub-standards associated with it that augment or extend it in important ways.

Design

VHDL is commonly used to write text models that describe a logic circuit. Such a model is processed bya synthesis program, only if it is part ofthe logic design. A simulation programis usedtotestthe logicdesignusingsimulationmodelsto representthe logic circuits that interface to the design. This collection of simulation models is commonly called a *testbench*.

VHDL has constructs to handle the parallelism inherent in hardware designs,but these constructs (processes) differ in syntax from the parallel constructs in Ada (tasks). Like Ada, VHDL is strongly typed and is not case sensitive. In order to directly represent operations which are common in hardware, there are many features of VHDL which are not found in Ada, such as an extended set of Boolean operators including nand and nor. VHDL also allows arrays to be indexed in either ascending or descendingdirection;both conventions are used in hardware, whereas in Ada and most programming languages only ascending indexing is available.

Advantages

The key advantage of VHDL, when used for systems design, is that it allows the behavior of the required system to be described (modeled) and verified (simulated) before synthesis tools translate the design into real hardware (gates and wires).

Anotherbenefit isthat VHDLallowsthedescriptionofa concurrent system. VHDLis a dataflow language, unlike procedural computing languages such as BASIC, C,and assembly code, which allrun sequentially, one instruction at a time.

AVHDLproject is multipurpose. Being created once, a calculationblock can be used in many other projects. However, many formational and functional block parameters can be tuned (capacity parameters, memory size, element base, block composition and interconnection structure).

Xilinx

Xilinx ISE[1] (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize ("compile") their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and configure the target device with the programmer.

Technology

The Spartan-3 platform was the industry's first 90nm FPGA, delivering more functionalityand bandwidthper dollar thanwas previouslypossible, setting new standards in the programmable logic industry.

Xilinx designs, develops and markets programmable logic products, including integrated circuits (ICs), software design tools, predefined system functions delivered as intellectual property (IP) cores, design services, customer training, field engineering and technical support. Xilinx sells both FPGAs and CPLDs for electronic equipment manufacturers in end markets such as communications, industrial,consumer,automotive and data processing.

Xilinx's FPGAs have been used for the ALICE (A Large Ion Collider Experiment) at the CERN European laboratory on the French-Swiss border to map and disentangle the trajectories ofthousands ofsubatomic particles. Xilinx has also engaged ina partnership with the United States Air Force Research Laboratory's Space Vehicles Directorate to develop FPGAs to withstand the damaging effects of radiation in space, which are 1,000 times less sensitive to space radiation than the commercialequivalent, for deployment in new satellites.

The Virtex-II Pro, Virtex-4, Virtex-5, and Virtex-6 FPGA families, which include up to two embedded IBM PowerPC cores, are targeted to the needs of system-on-chip (SoC) designers.

Xilinx FPGAs can run a regular embedded OS (such as Linux or vxWorks) and can implement processor peripherals in programmable logic.

Xilinx's IP cores include IP for simple functions (BCD encoders, counters, etc.), for domain specific cores (digital signal processing, FFT and FIR cores) to complex systems (multi-gigabit networking cores, the Micro Blaze soft microprocessor and the compact Picoblaze microcontroller). Xilinx also creates customcores for a fee.

The main design toolkit Xilinx provides engineers is the Vivado Design Suite, an integrated design environment (IDE) with a system-to-IC level tools built on ashared scalable data model and a common debug environment. Vivado includes electronic system level (ESL) design tools for synthesizing and verifying C-based algorithmic IP; standards based packaging of both algorithmic and RTL IP for reuse; standards based IP stitching and systems integration of all types of system building blocks; and the verification of blocks and systems. A free version WebPACK Edition of Vivado provides designers with a limited version of the design environment.

Xilinx's Embedded Developer's Kit (EDK) supports the embedded PowerPC 405 and 440 cores(inVirtex-II Pro and some Virtex-4 and -5 chips) and the Microblaze core. Xilinx's SystemGenerator for DSP implements DSP designs onXilinx FPGAs. A freeware versionof its EDA software called ISE WebPACK is used with some ofitsnon-high-performance chips. Xilinx is the only (as of 2007) FPGA vendor to distribute a native Linux freeware synthesis tool chain

IntroductiontoIRSIMandGOSPL(opensourcepackages).

IRSIM

IRSIM is a tool for simulating digital circuits. Itis a "switch-level" simulator; thatis, it treats transistors as ideal switches. Extracted capacitance and lumped resistance values are used to make the switch a little bitmore realistic than the ideal,using the RC time constants to predict the relative timing of events.

IRSIM shares a history with magic, although it is an independent program. Magic was designed to produce, and IRSIM to read, the ".sim" file format, which is largely unused outside of these two programs. IRSIM was developed at Stanford, while Magicwas developed at Berkeley. Parts of Magic were developed especially for use with IRSIM, allowing IRSIM to run a simulation in the "background" (i.e., a forked process communicating through a pipe), while displaying information about the values of signals directly on the VLSI layout.

For "quick" simulations of digital circuits, IRSIM is still quite useful for confirming basic operation of digital circuit layouts. The addition of scheduling commands("at","every", "when", and "whenever") put IRSIM into the same class as Verilog simulators. It is, in myopinion,mucheasier to write complicated testbenchsimulations using Tcland IRSIM.I have used IRSIM to validate the digital parts of several production chips at MultiGiG, including the simulation of analog behavior such as PLL locking.

IRSIM version 9.5 was a long-standing and stable version that corresponded to the relativelystableMagicversion6.5.Whenmagicwasrecast ina Tcl/Tk interpreterframework (versions 7.2 and 7.3), IRSIM could no longer operate as a background process. However, it was clear that if IRSIM could also be recast in the same Tcl/Tk interpreter framework, the level of interaction between it and Magic would be greatly increased.

Design verification and testing, simulation at various levelsincluding timing verification,faults models.

Designverification

Design verification is the most important aspect of the product development process illustratedin Figures , consuming as muchas 80%ofthetotalproduct development time. The intent is to verify that the design meets the system requirements and specifications. Approaches to design verification consist of (1) logic simulation/emulation and circuit simulation, in which detailed functionality and timing of the design are checked by means of simulation or emulation; (2) functional verification, in whichfunctional models describingthe functionality of the design are developed to check against the behavioral specification of the design without detailed timing simulation; and (3) formal verification, in which the functionalityischeckedagainsta—golden‖model.Formalverificationfurtherincludes

propertychecking (or modelchecking), inwhichthe propertyofthe design is checked against some presumed ―properties‖ specified in the functional or behavioral model (e.g., a finite-state machine should not enter a certain state), and equivalence checking, in which the functionalityis checked against a ―golden‖ model.

Simulation-based techniques are the most popular approach to verification, even though these are time-consuming and may be incompletein finding design errors. Logic simulationis used throughout every stage of logic design automation, whereas circuit simulation is used after physical design. The most commonly used logic simulation techniques are compiled-code simulation and event-driven simulation .The former is most effective for cyclebased two-valued simulation; the latter is capable of handling various gate and wire delay models. Although versatile and low in cost, logic simulation is too slow for complex SOC designs or hardware/software co-simulation applications. For more accurate timing information and dynamic behavior analysis, devicelevel circuit simulation is used. However, limited by the computation complexity, circuit simulation is, in general, only applied to critical paths, cell library components, and memory analysis.

Emulation-based verification by use of FPGAs provides an attractive alternative to simulation-based verification as the gap between logic simulation capacity and design complexity continues growing. Before the introduction of FPGAs in the 1980s, ASICs were often verified by construction of a breadboard by use of small-scale integration (SSI) and medium-scale integration (MSI) devices on a wire-wrap board. This becameimpractical as the complexity and scale of ASICs moved into the VLSI realm. As a result, FPGAs became the primary hardware for emulation-based verification. Although these approaches are costly and may not be easy to use, they improve verification time by two to three orders of magnitude compared with software simulation.

Formal verification techniques are a relatively new paradigm for equivalence checking. Instead of input stimuli, these techniques perform exhaustive proof through rigorous logical reasoning. The primary approaches used for formal verification include binary decision diagrams (BDDs) and Boolean satisfiability (SAT). These approaches, along with other algorithms specific to EDA applications. The BDD approach successively applies Shannon expansion onall variables ofa combinational logic function untileither the constant function ―0‖or―1‖isreached.

TESTAUTOMATION

Advances in manufacturing process technology have also led to verycomplex designs. Asa result, it has become a requirement that design-for-testability(DFT) featuresbe incorporated in the register-transfer level(RTL) or gatelevel design before physicaldesign to ensure the qualityofthe fabricated devices. In fact, thetraditionalVLSI development process illustrated in Figure involves some form of testing at each stage, includingdesignverification. Once verified, the VLSI design then goes to fabrication and,at the same time, test engineers develop a test procedure based on the design specification and fault models associated with the implementation technology. Because the resulting product quality is in general unsatisfactory, modern VLSI test development planning tends to start when the RTL design is near completion. This test development plan defines what test requirements the product must meet, often in terms of defect level and manufacturing yield, test cost, and whether it is necessaryto performself-test and diagnosis.

Faultmodels

A defect is a manufacturing flaw or physical imperfection that may lead to a fault, a fault can cause a circuit error, and a circuit error can resultin a failure of the device or system. Because of the diversity of defects, it is difficult to generate tests for real defects. Fault modelsare necessaryforgeneratingandevaluatingtest patterns.Generally,agoodfault model should satisfy twocriteria: (1) itshould accuratelyreflect the behavior ofdefects and
(2) it should be computationally efficient in terms of time required for fault simulation and test generation. Many fault models have been proposed but, unfortunately, no single fault model accurately reflects the behavior of all possible defects that can occur. As a result, a combination of different fault models is often used in the generation and evaluation of test patterns. Some well-known and commonly used fault models for general sequential logic include the following:

1. Gate-level stuck-at fault model: The stuck-at fault is a logical fault model that has been used successfully for decades.A stuck-at fault transforms the correct value on the faulty signal line to appear to be stuck-at a constant logic value, either logic 0 or 1, referred to as stuck-at-0(SA0)orstuck-at-1(SA1), respectively. This modelis commonlyreferredto asthe line stuck-at fault model where any line can be SA0 or SA1, and also referred to as the gate- level stuck-at faultmodelwhere any input or output ofanygate can be SA0 or SA1.

2. Transistor-level stuck fault model: At the switch level, a transistor can be stuck-off or stuck-on, also referred to as stuck-open or stuckshort, respectively. The line stuck-at fault model cannot accurately reflect the behavior of stuck-off and stuck-on transistor faults in complementary metal oxide semiconductor (CMOS) logic circuits because of the multiple transistors used to construct CMOS logic gates. A stuckopen transistor fault in a CMOS combinational logic gate can cause the gate to behave like a level-sensitive latch. Thus, a stuck-open fault in a CMOS combinational circuit requires a sequence of two vectors for 1.3 Test automation 19 detection instead of a single test vector for a stuck-at fault. Stuck-short faults, on the other hand, can produce a conducting path between power(VDD) and ground (VSS) and may be detected by monitoring the power supply current during steady state, referred to as IDDQ. This technique of monitoring the steady state power supply current to detect transistor stuck-short faults is called IDDQ testing.

3. Bridging fault models: Defects can also include opens and shorts in the wires that interconnect the transistors that form the circuit.Opens tend to behave like line stuck-at faults. However, a resistive open does notbehave the same as a transistor or line stuck-at fault, butinstead affects the propagation delayof the signalpath. A short between two wires is commonly referred to as a bridging fault. The case ofa wire being shorted to VDDor VSS is equivalent to the line stuck-at fault model. However, when two signal wires are shorted together, bridging fault models are needed; the three most commonly used bridging fault models

Designstrategiesfortesting chipleveland systemleveltesttechniques.

CHIP-LEVELTESTTECHNIQUES

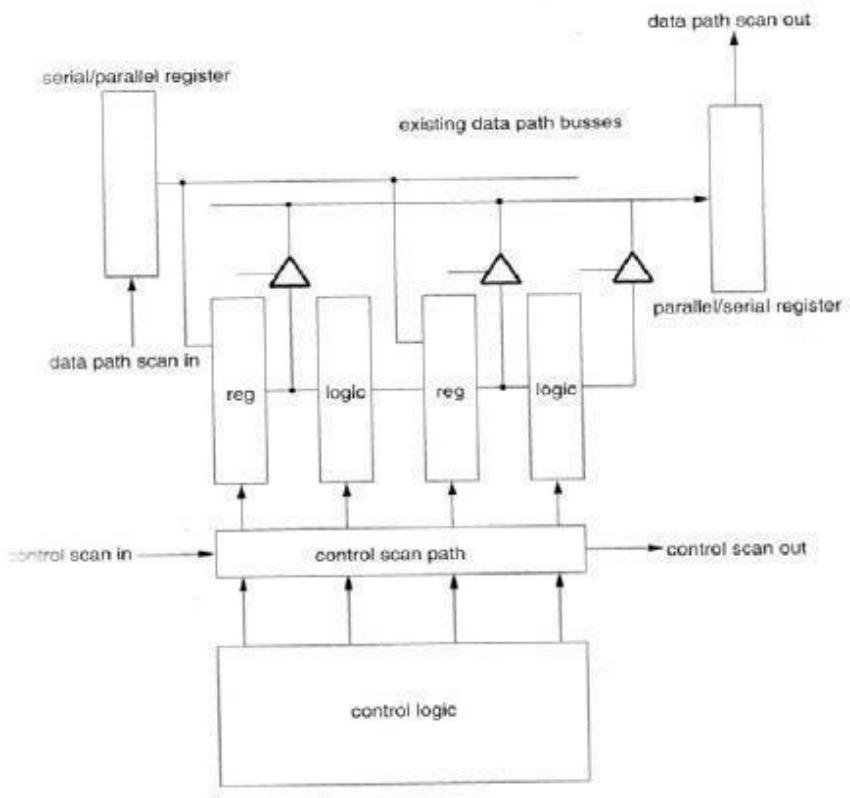
In the past the design process was frequently divided between a designerwho designed the circuit and a test engineer who designed the test to apply to that circuit. The advent of the ASIC, small design teams, the desire for reliable ICs and rapid times to market haveallforcedthe ―test problem‖earlier inthedesigncycle. Infact,thedesignerwho isonly thinking about what functionality has to be implemented and not about howto test the circuit will quite likely cause product deadlines to be slipped and in extreme cases precuts to be stillborn. In this section some practical methods of incorporating test requirements into a design. This discussion is structured around the main types of circuit structure that will been countered in a digital CMOS chip

RegularLogicArray

Partial serial scan or parallel scan is probably the best approach for structure such as dat a paths. One approach that has been used in a Lisp microprocessor is shown in figure . Here the input busses may be driven by a serially loaded register. These in turn may be sourced onto a bus, and this bus may be loaded into a register that may be serially accessed. Allofthe controlsignals to the data path are also made scannable

Memories

Memoriesmayusetheself-testingtechniquesmentionedinsection 5.3.4.2.alternatively, the provision of multiplexers on data inputs and addresses and convenient external access to data outputs enables the testing of embedded memories. It is a mistake to have memories indirectlyaccessible (i.e., data is written bypassing through logic, data is observed after passing through logic, addresses cannot be conveniently sequenced). Because memories have to be tested exhaustively, any overhead on writing and reading the memories can substantially increase the test time and, probably more significantly, turn the testing task into an effort inscrutability



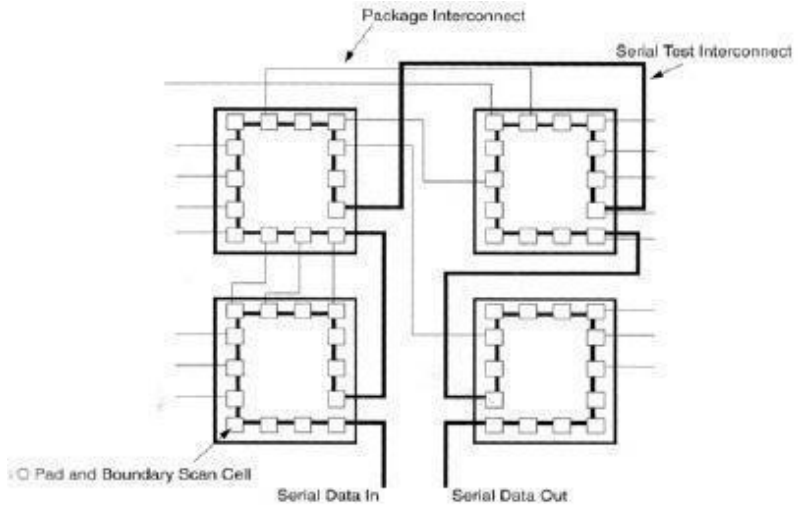
SYSTEM-LEVELTESTTECHNIQUES

Traditionallyat the board level, ―bed-of-nails‖ testers have been used to test boards. In this type of a tester, the board under test is lowered onto a set of test points that probe pointsofinterest ontheboard. These may besensed and drivento test thecompleteboard. At the chassis level, software programs are frequently used to test a complete board set. For instance, when a computer boots, it might run a memory test on the installedmemory to detect possible faults. The increasing complexityofboardsandthe movement totechnologies like Multichip Modules (MCMs) and surface-mount technologies resulted insystemdesigners agreeing on a unified scan-based methodology for testing chips at the board(and system level). This is called Boundary Scan

BoundaryScan

Introduction

The IEEE 1149 BoundaryScanarchitecture is shown in figure. In essence itprovides a standardized serial scan path through the I/O pins of an IC. At the board level, ICs obeying the standard may be connected in a variety of series and parallel combinations to enable testing ofa complete board or, possibly, collection of boards. The description here is a précis of the published standard .The standard allows for the following types of tests to be run in a unified testing framework



TheTestAccessPort (TAP)

TheTest AccessPort (TAP) isadefinitionofthe interfacethat needsto be included inanICto make it capable of being included in a Boundary-Scan architecture. The port has four or five single-bit connections, as follows

TCK (The Test Clock Input) – used to clock tests into and out of chips.

TMS (The Test Mode Select) –used to controltest operations.

TDI(The TestdataInput)–usedtoinputtestdatato achip.

TDO(the TestData Output)–usedtooutputtestdatafromachip.Italsohasanoptionalsignal

TRST (The Test Reset Signal) used to asynchronously reset the TAP controller, also used if a power-up reset signal is not available in the chip being tested. The TDO signal is defined as a tri-state signalthat is only driven when the TAP controller is outputting test data

The TDO signal is defined as a tri-state signal that is only driven when the TAP controller is outputting test data.

TheTestArchitecture

The basic test architecture that must be implemented on a chipis shown infigure5.25itconsistsof:

TAP interface pins a set of test- data registers to collect data from the chip an instruction register to enable test inputs to be applied to the

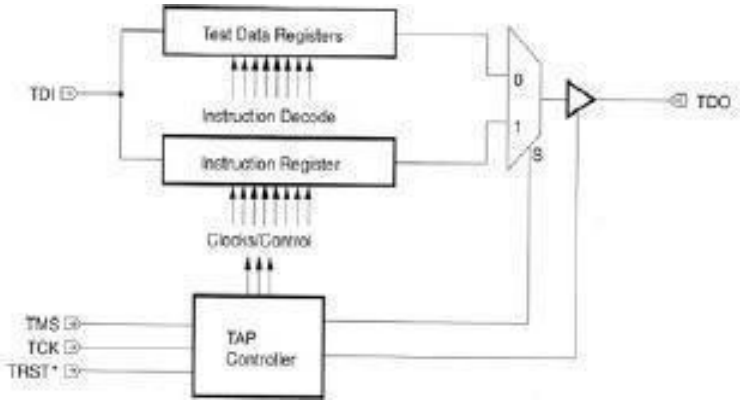


Figure5.25TAParchitecture

chip a TAP controller, which interpretstest instructions and controls the flow ofdataonto and outoftheTAP.Datathat is input viatheTDI portmaybe fedtooneor moretest dataregisters or an instruction register. An outputMUX selects betweentheinstructionregister and the data registers to be output to the tri-state TDO pin.

UNIT-6

INTRODUCTIONTOEMBEDDEDSYSTEM

EMBEDDEDSYSTEMOVERVIEW:-

- Computing systems are everywhere. There is no surprise that millions of computing systems are built every year destined for desktop computers (Personal Computers, or PC's), workstations, mainframes and servers.
- The billions of computing systems are built every year for a very different purpose: they are embedded within larger electronic devices, repeatedly carrying out a particular function, often going completely unrecognized by the device's user.
- An embedded system is nearly any computing system other than a desktop, laptop, or mainframe computer.

Shortlistofembeddedsystems:-

- Embeddedsystemsarefoundinavarietyofcommonelectronicdevices,suchas:
    1. **consumer electronics** -- cell phones, pagers, digital cameras, camcorders, videocassette recorders, portable video games, calculators, and personal digital assistants;
    2. **home appliances** -- microwave ovens, answering machines, thermostat, home security, washing machines, and lighting systems;
    3. **officeautomation**--faxmachines,copiers,printers,and scanners;
    4. **business equipment** -- cash registers, curbside check-in, alarm systems, card readers, product scanners, and automated teller machines;
    5. **automobiles** -- transmission control, cruise control, fuel injection, anti-lock brakes, and active suspension.

Characteristicsofembeddedsystems:-

- Embeddedsystemshaveseveralcommoncharacteristics:

1) **Single-functioned:** Anembedded systemusuallyexecutes onlyone program, repeatedly. For example, apager isalwaysapager. Adesktopsystemexecutesavarietyofprograms, like spreadsheets, word processors, and video games, with new programs added frequently.
2) **Tightly constrained:** All computing systems have constraints on design metrics.A design metric is a measure of an implementation's features, such as cost, size, performance, and power. Embedded systems often must cost just a few dollars, must be sized to fit on a single chip, must perform fast enough to process data in real-time, and must consume minimumpower toextend batterylifeor prevent thenecessityofacooling fan.

3) **Reactive and real-time:** Many embedded systems must continually react to changes in the system's environment, and must compute certain results in real time without delay. For example, a car's cruise controller continually monitors and reacts to speed and brake sensors. It must compute acceleration or decelerations amounts repeatedly within a limited time; a delayed computation result could result in a failure to maintain controlof the car. A desktop system typically focuses on computations, with relatively infrequent (fromthe computer's perspective) reactions to input devices. Inaddition, a delay in those computations, while perhaps inconvenient to the computer user, typically does not result in a system failure.

ADIGITALCAMERA:-

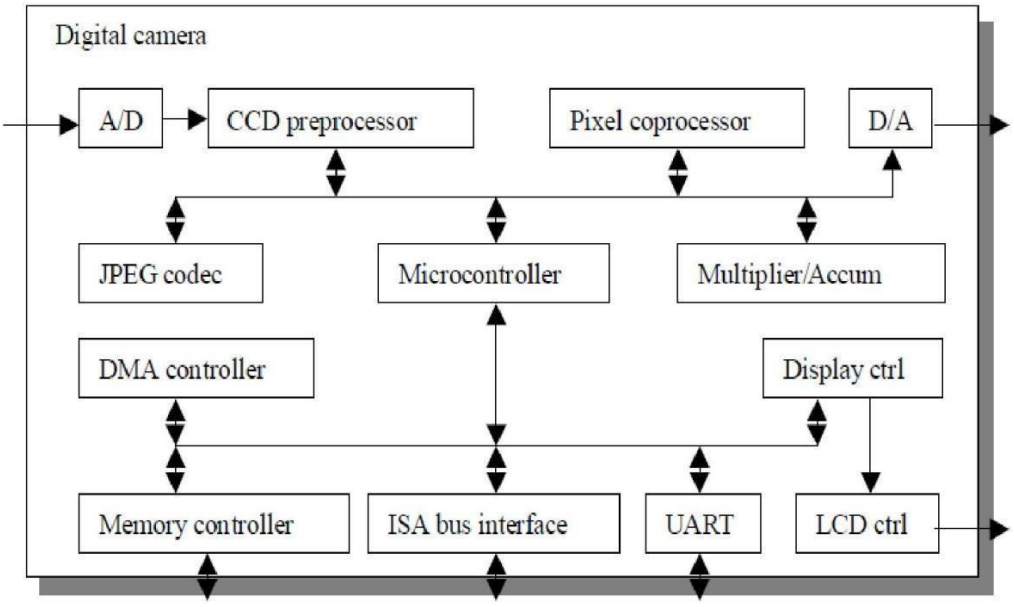
Considerthe digitalcamerasystemasshowninthebelowfigure.

- The **A2D** and **D2A** circuits convert analog images to digital and digital to analog, respectively.
- The**CCDpreprocessor**isacharge-coupleddevicepreprocessor.
- The **JPEG codec** compresses and decompresses an image using the JPEG2 compression standard, enabling compact storage in the limited memoryofthe camera.
- The**Pixelcoprocessor**aidsinrapidlydisplayingimages.
- The **Memory controller** controls access to a memory chip also found in the camera, while the **DMAcontroller**enablesdirect memoryaccesswithout requiring the useofthe microcontroller.
- The **UART** enables communication with a PC's serial port for uploading video frames, while the **ISA bus interface** enables a faster connection witha PC's ISAbus.
- The **LCD ctrl** and **Display ctrl** circuits control the display of images on the camera's liquid-crystal display device.
- A**Multiplier/Accum**circuitassistswithcertaindigitalsignalprocessing.
- The heart of the system is a **microcontroller**, which is a processor that controls the activities of all the other circuits. Each device as a processor designed for a particular task, while the microcontroller is a more generalprocessor designed for generaltasks.

Thisexampleillustratessomeoftheembeddedsystemcharacteristicsdescribed above.

- It performs a single function repeatedly. The system always acts as a digital camera, wherein itcaptures, compresses and stores frames, decompresses and displays frames, and uploads frames.
- It is tightly constrained. The system must be low cost since consumers must be able to afford such a camera. It must be small so that it fits within a standard-sized camera. It must be fast so that it can process numerous images in milliseconds. It must consumelittle power so that the camera's batterywill last a long time.

- This particular system does not possess a high degree of the characteristic ofbeing reactive and real-time, as it only needs to respond to the pressing of buttons by a user, whicheven for anavid photographer is stillquite slow withrespect to processorspeeds.



Anembeddedsystemexample--adigitalcamera.

EMBEDDEDSYSTEMSTECHNOLOGIES:-

- Technologyasamannerofaccomplishingatask,especiallyusingtechnicalprocesses, methods, or knowledge.
- Therearethreetechnologies intheembeddedsystemdesign:
  1. Processortechnologies
  2. ICtechnologies
  3. Designtechnologies

PROCESSORTECHNOLOGY:-

GeneralPurposeProcessors---Software:-

- Thegeneral-purposeprocessorbuildsadevicesuitable for avarietyofapplications,to maximize the number of devices sold.
- One featureofsuchaprocessorisaprogrammemory–thedesigner doesnot knowwhat programwillrunontheprocessor, sotheprogramcannot bebuild intothedigitalcircuit.
- Anotherfeatureisageneraldatapath–thedatapathmust begeneralenoughto handlea varietyof computations, so typically has a large register file and one or more general-purpose arithmetic-logic units (ALUs).
- Anembeddedsystemsimplyusesageneral-purposeprocessor, byprogrammingthe processor's memoryto carryout the required functionality.

- Usingageneral-purposeprocessorinanembedded systemmayresult inseveraldesign-metric benefits.
    1. **Designtime**and**NRE***cost*are low,becausethedesigner mustonlywritea program, but need not do anydigital design.
    2. **Flexibility**ishigh,becausechanging functionalityrequiresonlychanging the program.
    3. **Unitcost**mayberelativelylow insmallquantities, sincetheprocessor manufacturer sells large quantities to other customers.
    4. **Performance** maybe fast for computation-intensiveapplications, ifusingafast processor,dueto advancedarchitecturefeaturesand leadingedgeICtechnology.
- Thereare also somedesign-metricdrawbacks.
    a. **Unitcost**maybetoohighforlargequantities.
    b. **Performance**maybeslowfor certainapplications.
    c. **Size** and **power** may be large due to unnecessary processor hardware.

Figure1(b) illustratesthatageneral-purposecoversthedesiredfunctionality, butnot necessarily efficiently.

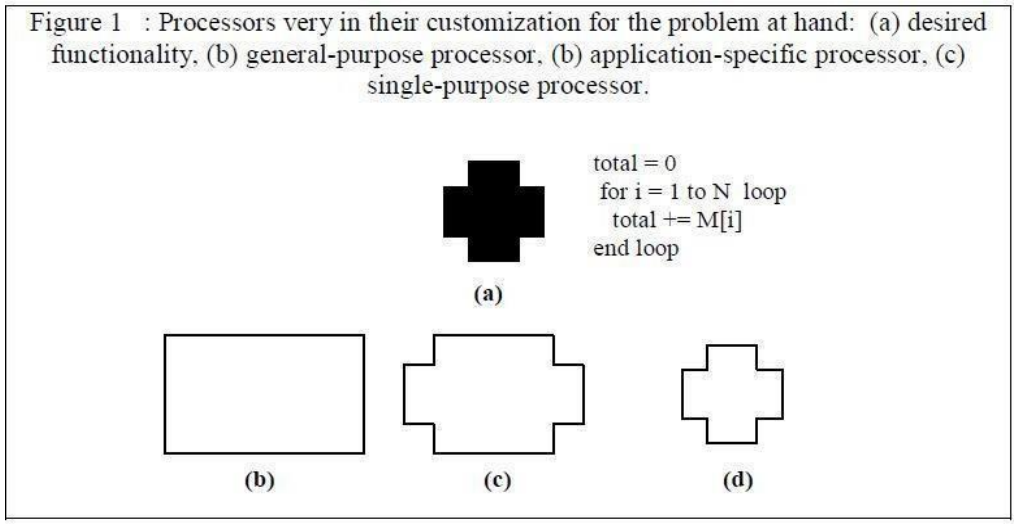
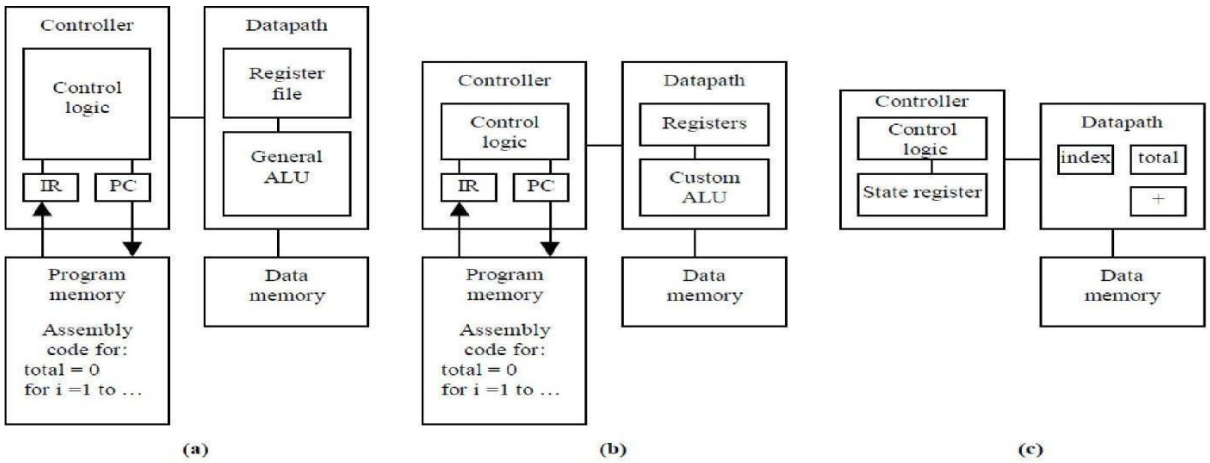


Figure 1 : Processors very in their customization for the problem at hand: (a) desired functionality, (b) general-purpose processor, (b) application-specific processor, (c) single-purpose processor.

Figure 2(a) shows a simple architecture of a general-purpose processor implementing the array summing functionality. The functionality is stored in a program memory. The controller fetches thecurrent instruction,asindicatedbytheprogramcounter(PC),intotheinstructionregister(IR). It then configures the datapath for this instruction and executes the instruction. Finally, it determinesthe appropriate next instructionaddress, setsthe PCtothisaddress, and fetchesagain.

Figure2:

Implementing desired functionality on different processor types: (a) general-purpose, (b) application-specific, (c) single-purpose.



SinglePurposeProcessors ------ Hardware:-

- A single-purpose processor is a digital circuit designed to execute exactly one program. For example, consider the digital camera. All of the components other than the microcontroller are single-purpose processors. The JPEG codec, for example, executes a single programthat compresses and decompresses videoframes.
- An embedded system creates a single-purpose processor by designing a custom digital circuit.
- Using a single-purpose processor in an embedded systemresults in severaldesign metric benefits and drawbacks, which are essentially the inverse of those for general purpose processors.
- Performance may be fast, size and power may be small, and unit-cost may be low for large quantities, while design time and NRE costs may be high, flexibility is low, unitcost may be high for small quantities, and performance may not match general-purpose processors for some applications.

Forexample, Figure1(d)illustratestheuseofa single-purposeprocessorinourembeddedsystem example, representing an exact fit ofthe desired functionality. Figure 2(c) illustratesthe architecture of such a single-purpose processor for the example. Since the example counts from one to N, we add an index register. The index register will be loaded with N, and willthen count downto zero,at whichtime it willassert astatuslinereadbythecontroller. Theexample hasonly one other value, we add onlyone register labeled totalto the datapath. Since the example's only arithmetic operation is addition, we add a single adder to the datapath. Since the processor only executesthis one program, we hardware the programdirectly into the control logic.

APPLICATION--SPECIFICPROCESSORS:-

- Anapplication-specificinstruction-set processor(orASIP)canserveasacompromise between the other processor.
- AnASIPisdesigned foraparticularclassofapplicationswithcommoncharacteristics, such as digital-signal processing, telecommunications, embedded control, etc.
- AnASIP inanembeddedsystemcanprovidethebenefit offlexibilitywhilestill achieving good performance, power and size.
- SuchprocessorscanrequirelargeNREcosttobuildtheprocessoritself.

Microcontrollers:-

- A microcontroller is a microprocessor that has been optimized for embedded control applications.
- Suchapplicationstypicallymonitorandset numeroussingle bit controlsignals but do not perform large amount of data computations. Thus microcontrollers tend to have simple datapaths that excel bit-level operations and reading and writing external bits.
- Furthermore, they tend to incorporate on the microprocessor chip several peripheral components common in control applications like serialcommunicationperipherals, times, counters, pulse width modulators and analog to digital converters. Such incorporation of peripherals enables single chip implementations and hence smaller and lower cost product.

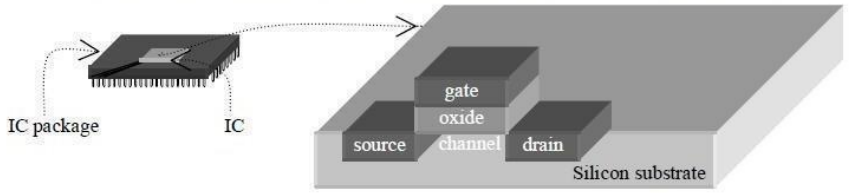
DigitalSignalProcessing:-

- Digital-signalprocessors(DSPs)areacommonclassofASIP.
- A DSP is a processor designed to perform common operations on digital signals, which are the digital encodings of analog signals like video and audio. These operations carry out common signalprocessing tasks like signal filtering, transformation, orcombination.
- Suchoperationsare usually math-intensive, including operations like multiplyand add or shift and add.
- To support suchoperations, a DSP may have specialpurpose datapath components sucha multiply-accumulate unit, which can perform a computation like T = T + M[i]*k using only one instruction.
- Figure 1(c) illustrates the use of an ASIP ; while partially customized to the desired functionality, there is some inefficiency since the processor also contains features to support reprogramming.
- Figure 2(b) shows the generalarchitecture of an ASIP. The datapath may be customized. It may have an auto-incrementing register, a path that allows the add of a register plus a memory location in one instruction, fewer registers, and a simpler controller.

ICTECHNOLOGY:-

- EveryprocessormusteventuallybeimplementedonanIC.
- AnIC(IntegratedCircuit),oftencalleda"chip," is asemiconductordeviceconsistingof a set of connected transistors and other devices.
- Anumberofdifferent processesexistto buildsemiconductors,the most popularofwhich is CMOS (Complementary Metal Oxide Semiconductor).
- Semiconductorsconsist ofnumerouslayersasshowninthefiguregiven below.

Figure : IC's consist of several layers. Shown is a simplified CMOS transistor; an IC may possess millions of these, connected by layers of metal (not shown).



- Thebottomlayers formthetransistors. Themiddle layers formlogicgates. Thetoplayers connect these gates with wires. These layers can be created bydepositing photo-sensitive chemicals on the chip surface and then shining light through masks to change regions of the chemicals. A set of masks is often called a layout. The narrowest line that we can create on a chip is called the feature size.

FullCustom/VLSI:-

- In a full-custom IC technology, we optimize all layers for our particular embedded system's digital implementation.
- Such optimization includes placing the transistors to minimize interconnection lengths, sizing the transistors to optimize signal transmissions and routing wires among the transistors.
- Once all the masks are completed, then we send the mask specifications to a fabrication plant that builds the actual ICs.
- Full-custom IC design, often referred to as VLSI (Very Large Scale Integration) design, has very high NRE cost and long turnaround times (typically months) before the IC becomes available, but can yield excellent performance with small size andpower.
- Itisusuallyusedonlyinhigh-volumeorextremelyperformance-criticalapplications.

SemicustomASIC(GateArray and StandardCell):-

- In an ASIC (Application-Specific IC) technology, the lower layers are fully or partially built, leaving us to finish the upper layers.

- Inagatearraytechnology, themasks forthetransistorandgatelevelsarealready built (i.e., the IC already consists of arrays ofgates).
- Theremainingtaskistoconnectthesegatestoachieveourparticularimplementation.
- Inastandard celltechnology,logic-levelcells(suchasanANDgateoranAND- OR-INVERT combination) have their mask portions pre-designed, usually by hand.
- Thus,theremainingtask isto arrangetheseportionsinto completemasksforthe gate level, and then to connect the cells.
- ASICsarebyfarthemost popular ICtechnology, astheyprovide forgood performance and size, with much less NRE cost than full-customIC's.

PLD:-

- Ina PLD(Programmable Logic Device) technology, layers implement aprogrammable circuit, where programming has a lower-level meaning than a software program.
- The programming that takes place may consist of creating or destroying connections between wires that connect gates, either by blowing a fuse, or setting a bit in a programmable switch.
- Small devices, called programmers, connected to a desktop computer can typically perform such programming.
- PLD's of two types, simple and complex. One type of simple PLD is a PLA (Programmable Logic Array), which consists of a programmable array of AND gates and a programmable array of OR gates.
- Anothertype isaPAL(Programmable ArrayLogic),whichuses just oneprogrammable arrayto reduce the number of expensive programmable components.
- One type of complex PLD, growing very rapidly in popularity over the past decade, is the FPGA (Field Programmable Gate Array), which offers more general connectivity among blocks of logic, rather than just arrays of logic as with PLAs and PALs, and are thus able to implement far more complex designs. PLDs offer very low NRE cost and almost instant IC availability.
- They are typically bigger than ASICs, may have higher unit cost, may consume more power, and may be slower (especially FPGAs). They still provide reasonable performance, though, so are especiallywell suited to rapid prototyping.