

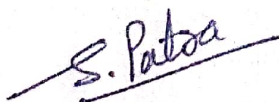
C.V. RAMAN POLYTECHNIC BBSR

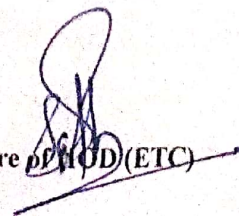


LESSON PLAN

Discipline: Diploma Branch: EE	Semester: 5 th	Name of the Teaching Faculty: Sabyasachi Patra
Subject: Digital Electronics & Microprocessor (TH-3)	No. of Days/per week class allotted: 75days/ 5 class per week	Semester From Date: 14/07/2025 To Date: 15/11/2025 No. of Weeks: 15
Week	Class Day	Theory
1 st	1 st	1.1 Number systems and Decimal comparison
	2 nd	1.2 Binary addition, subtraction, multiplication, division
	3 rd	1.3 1's and 2's complements
	4 th	1.4 Subtraction using 2's complement
	5 th	1.5 Weighted/Unweighted codes: 8421, Excess-3, Gray
2 nd	1 st	1.5 Code conversions
	2 nd	1.6 Parity Bit importance
	3 rd	1.7 Logic Gates and truth tables
	4 th	1.8 NAND/NOR gate realization
	5 th	1.9 Boolean Algebra and DeMorgan's Theorem
3 rd	1 st	1.10 Logic simplification using Boolean Algebra
	2 nd	1.11 K-Map (2,3,4 var), SOP & POS
	3 rd	2.1 Combinational logic concept
	4 th	2.2 Half adder & truth table
	5 th	2.3 Half adder using NAND/NOR only
4 th	1 st	2.4 Full adder & truth table
	2 nd	2.5 Full adder using Half adders + OR
	3 rd	2.6 Full subtractor & truth table
	4 th	2.7 4×1 MUX and 1×4 DEMUX
	5 th	2.8 Binary-Decimal Encoder & 3×8 Decoder
5 th	1 st	2.9 2-bit Magnitude Comparator
	2 nd	3.1 Sequential logic circuits intro
	3 rd	3.2 Clock necessity, level vs edge trigger
	4 th	3.3 Clocked SR FF with preset/clear
	5 th	3.5 JK FF using SR FF
6 th	1 st	3.6 Race condition & Master-Slave JK FF
	2 nd	3.7 Truth tables for D & T FFs
	3 rd	3.8 Flip flop applications
	4 th	3.9 Modulus of counter
	5 th	3.10 4-bit asynchronous counter
7 th	1 st	3.11 Asynchronous decade counter
	2 nd	3.12 4-bit synchronous counter
	3 rd	3.13 Sync vs Async counters
	4 th	3.14 Need for Registers, types

8 th	5 th	3.15 SISO, SIPO, PISO, PIPO operation
	1 st	4.1 Microprocessor & Microcomputer intro
	2 nd	4.2 8085 Architecture description
	3 rd	4.3 Pin diagram & description
	4 th	4.4 Stack, Stack pointer, Stack top
9 th	5 th	4.5 Interrupts, 4.6 Opcode & Operand
	1 st	Class Test-1
	2 nd	4.7 One/two/three byte instructions
	3 rd	4.8 Instruction set examples
	4 th	4.9 Addressing modes
10 th	5 th	4.10 Fetch, machine, instruction cycles
	1 st	4.11 Timing diagrams (memory read/write, I/O)
	2 nd	4.12 Instruction timing diagram
	3 rd	4.13 Counters and delay programs
	4 th	4.14 Assembly programming basics
11 th	5 th	4.14 Example programs in 8085
	1 st	5.1 Interfacing, memory and I/O mapping
	2 nd	5.2 Intel 8255 block diagram
	3 rd	5.2 8255 description of blocks
	4 th	5.3 8255 app: 7-segment display
12 th	5 th	5.3 8255 app: Square wave gen.
	1 st	5.3 8255 app: Traffic light controller
	2 nd	Revision: Unit 1 Concepts
	3 rd	Revision: Unit 2 Circuits
	4 th	Revision: Unit 3 Flip-Flops & Counters
13 th	5 th	Revision: Unit 4 Microprocessor
	1 st	Revision: Unit 5 Interfacing
	2 nd	Previous Year Question Discussion
	3 rd	Class Test - 2
	4 th	Doubt Clearing - Logic & K-map
14 th	5 th	Doubt Clearing - Counters & Registers
	1 st	Doubt Clearing - Instruction Sets
	2 nd	Extra: Gate-Level Design Tasks
	3 rd	Extra: ALP coding practices
	4 th	Extra: 8085 Instruction simulation
15 th	5 th	Practice: K-Map & Boolean Laws
	1 st	Practice: FFs & Timing Diagrams
	2 nd	Practice: Addressing & Opcode Types
	3 rd	Quiz Test
	4 th	Final Revision & Recap
	5 th	Remedial Class


Signature of Faculty


Signature of HOD(ETC)