C.V. RAMAN POLYTECHNIC BBSR

LESSON PLAN

Discipline: Diploma Branch: EE	Semester: 5th	Name of the Teaching Faculty: Sabyasachi Patra
Subject: Digital Electronics & Microprocessor (TH-3)	No. of Days/per week class allotted: 75days/ 5 class per week	Semester From Date: 14/07/2025 To Date:15/11/2025 No. of Weeks:15
Week	Class Day	Theory
1st	1st	1.1 Number systems and Decimal comparison
	2nd	1.2 Binary addition, subtraction, multiplication, division
	3rd	1.3 1's and 2's complements
	4th	1.4 Subtraction using 2's complement
	5th	1.5 Weighted/Unweighted codes: 8421, Excess-3, Gray
2nd	1st	1.5 Code conversions
	2nd	1.6 Parity Bit importance
	3rd	1.7 Logic Gates and truth tables
	4th	1.8 NAND/NOR gate realization
	5th	1.9 Boolean Algebra and DeMorgan's Theorem
3rd	1st	1.10 Logic simplification using Boolean Algebra
	2nd	1.11 K-Map (2,3,4 var), SOP & POS
	3rd	2.1 Combinational logic concept
	4th	2.2 Half adder & truth table
	5th	2.3 Half adder using NAND/NOR only
4th	1st	2.4 Full adder & truth table
	2nd	2.5 Full adder using Half adders + OR
	3rd	2.6 Full subtractor & truth table
	4th	2.7 4×1 MUX and 1×4 DEMUX
	5th	2.8 Binary-Decimal Encoder & 3×8 Decoder
5th	1st	2.9 2-bit Magnitude Comparator
	2nd	3.1 Sequential logic circuits intro
	3rd	3.2 Clock necessity, level vs edge trigger
	4th	3.3 Clocked SR FF with preset/clear
	5th	3.5 JK FF using SR FF
6th	1st	3.6 Race condition & Master-Slave JK FF
	2nd	3.7 Truth tables for D & T FFs
	3rd	3.8 Flip flop applications
	4th	3.9 Modulus of counter
	5th	3.10 4-bit asynchronous counter
7th	1st	3.11 Asynchronous decade counter
	2nd	3.12 4-bit synchronous counter
	3rd	3.13 Sync vs Async counters
	4th	3.14 Need for Registers, types

	5th	3.15 SISO, SIPO, PISO, PIPO operation
8th	1st	4.1 Microprocessor & Microcomputer intro
	2nd	4.2 8085 Architecture description
	3rd	4.3 Pin diagram & description
	4th	4.4 Stack, Stack pointer, Stack top
	5th	4.5 Interrupts, 4.6 Opcode & Operand
9th	1st	Class Test-1
	2nd	4.7 One/two/three byte instructions
	3rd	4.8 Instruction set examples
	4th	4.9 Addressing modes
	5th	4.10 Fetch, machine, instruction cycles
10th	1st	4.11 Timing diagrams (memory read/write, I/O)
	2nd	4.12 Instruction timing diagram
	3rd	4.13 Counters and delay programs
	4th	4.14 Assembly programming basics
	5th	4.14 Example programs in 8085
11th	1st	5.1 Interfacing, memory and I/O mapping
	2nd	5.2 Intel 8255 block diagram
	3rd	5.2 8255 description of blocks
	4th	5.3 8255 app: 7-segment display
	5th	5.3 8255 app: Square wave gen.
12th	1st	5.3 8255 app: Traffic light controller
	2nd	Revision: Unit 1 Concepts
	3rd	Revision: Unit 2 Circuits
	4th	Revision: Unit 3 Flip-Flops & Counters
	5th	Revision: Unit 4 Microprocessor
13th	1st	Revision: Unit 5 Interfacing
	2nd	Previous Year Question Discussion
	3rd	Class Test – 2
	4th	Doubt Clearing – Logic & K-map
	5th	Doubt Clearing – Counters & Registers
14th	1st	Doubt Clearing – Instruction Sets
	2nd	Extra: Gate-Level Design Tasks
	3rd	Extra: ALP coding practices
	4th	Extra: 8085 Instruction simulation
	5th	Practice: K-Map & Boolean Laws
15th	1st	Practice: FFs & Timing Diagrams
	2nd	Practice: Addressing & Opcode Types
	3rd	Quiz Test
	4th	Final Revision & Recap
	5th	Remedial Class

S. Patra

Signature of Faculty

Signature of HOD (ETC)