5TH SEM. / ETC & COMM. / E&TC/ 2023(W) NEW

Th-2 VLSI & Embedded System

Full Marks: 80 **Time- 3 Hrs**

Answer any five Questions including Q No.1& 2
Figures in the right hand margin indicates marks

1. Answer **All** questions 2 x 10
   a. Draw the symbol of PMOS and NMOS. Indicate the terminals.
   b. State Moore's Law.
   c. List any four VLSI design styles.
   d. Define photolithography in fabrication process.
   e. Write any two differences between positive and negative photo resist.
   f. Draw the stick diagram of CMOS inverter.
   g. Implement a AND gate using CMOS transmission gate(pass transistor logic).
   h. Draw the circuit diagram of an inverter designed using NMOS-Enhancement type load.
   i. Write the full form of the following
      a. VHDL
      b. FPGA
      c. ASIC
      d. EDA tool.
   j. Define Embedded System.

2. Answer **Any Six** Questions 6 x 5
   a. Explain the different regions of operations of N-MOSFET.
   b. Explain the VLSI Design hierarchy.
   c. Write a short note on various steps of VLSI fabrication process.
   d. With a neat circuit diagram, explain the working of resistive load inverter and draw its voltage transfer characteristics.
   e. Implement two input NAND and NOR gates using CMOS.
   f. Differentiate between DRAM and SRAM.(any 5)
   g Write a short note on how embedded system is used in DSP (Digital Signal Processor).

3 With a neat flow chart, explain the VLSI Design flow. 10

4 With neat diagrams, Explain the n-well CMOS fabrication process. 10

5 Implement a SR Latch using CMOS inverter and explain its working. 10

6 Write a short note on: 10
   a)FPGA [5]
   b)DRAM [5]

7 With a neat block diagram , explain the working of a digital camera. 10