5^{TH} SEM. / ETC & COMM. / ETC. & TELECOM. / 2022(W)

Th-2 VLSI & Embedded System

Full Marks: 80 Time- 3 Hrs

Answer any five Questions including Q No.1& 2
Figures in the right-hand margin indicates marks

1. Answer **All** questions. 2 x 10

a. Define pinch off voltage of an NMOS transistor.

b. Name the two lay out design rules of VLSI.

c. Define noise margins (NM_L and NM_H) of a CMOS inverter.

d. Implement XNOR gate using pass transistors.

e. Write the full forms of the following.
1. ULSI 2. EDA 3. VHDL 4. PLD

f. Define propagation delay of a CMOS inverter.

g. Number of transistors per chip ____ and minimum feature size ____with the evolution in VLSI technology. (Increases, decreases)

h. Given $\boldsymbol{v_{GS} = 1.2V, V_{TN} = 0.6V, v_{DS} = 0.9V}$. Calculate overdrive voltage ($\boldsymbol{v_{OV}}$) and mention the region of operation of NMOS transistor.

i. What are the basic characteristics of an embedded system?

j. Find/Derive the condition for symmetric delay of a static CMOS inverter.

2. Answer **Any Six** Questions 6 x 5

a. Given $\boldsymbol{\mu_n C_{OX} = 160 \frac{\mu A}{V^2}}$, $\boldsymbol{W = 0.36\mu m}$, $\boldsymbol{L = 0.18\mu m}$, $\boldsymbol{V_{TN} = 0.4V}$. Consider NMOS transistor. For $\boldsymbol{v_{GS} = 0.6}$, $\boldsymbol{v_{DS} = 1.0V}$, indicate the region of operation of the transistor, and calculate the drain current i_D.

b. Realize a NOR2 gate using static CMOS and explain its working.

c. Design a clocked D latch using static CMOS.

d. What is FPGA? Explain its architecture with neat diagram.

e. Differentiate between SRAM and DRAM.

f. Draw the stick diagram and lay out for static NAND2 gate.

g Find the worst-case Elmore parasitic delay of an n-input NAND gate.

3	Draw the steps for VLSI fabrication of an NMOS transistor.	10
4	Explain the construction and working of an enhancement type NMOS transistor and plot the graph between i_D and v_{DS}.	10
5	Explain the working of digital camera with the help of block diagram.	10
6	Describe VLSI design methodology, design flow and Y chart.	10
7	Implement full adder using static CMOS.	10