

**3RD SEM./ AE & IE /CSE /EE(I& C) / ETC & COMM./
ETC & TELECOMM./ IT/ MECHATRONICS/ 2022(W)**

Th-3 Digital Electronics

Full Marks: 80

Time- 3 Hrs

Answer any five Questions including Q No.1& 2
Figures in the right hand margin indicates marks

1. Answer **All** questions 2 x 10
 - a. Define Racing conditions.
 - b. Convert the decimal number $(1000)_{10}$ into hexadecimal.
 - c. Write down the difference between synchronous and asynchronous Counter.
 - d. Design a Half adder using basic logic gates.
 - e. Perform 2's complement subtraction of $1000011 - 1010111$.
 - f. What is difference between weighted and non-weighted binary code?
 - g. What is Max term and Min term?
 - h. State two difference between counter and register.
 - i. Write down the truth table of Exclusive-NOR gate.
 - j. Convert $(101011110.1011)_2$ to Octal and hexadecimal number.

2. Answer **Any Six** Questions 6 x 5
 - a. Which gates are referred as universal gates and why? How other gates can be realized using NAND gate?
 - b. Design an 8:3 Encoder with neat circuit diagram.
 - c. Distinguish between combinational and sequential logic circuit.
 - d. Describe the operation of full subtractor with the help of truth table and circuit diagram.
 - e. Convert D-type flip flop to SR flip flop.
 - f. Explain the operation of seven segments displays.
 - g. Design a 2 bit magnitude comparator circuit for whose outputs are $A > B$, $A < B$ and $A = B$ where A and B are 2 bits binary numbers

- 3 Define SOP and POS term. Obtain the canonical SOP and POS form and draw the truth table of the given function. 10
 $Y(A,B,C)=A+\overline{BC}$
- 4 What is shift register? Explain the working of SISO and PISO register with the help of suitable logic diagram 10
- 5 Sketch the logic diagram of clocked JK flip flop. Explain its working with the functional table. 10
- 6 With neat circuit diagram explain the function of 4:1 multiplexer and 1:4 demultiplexer. 10
- 7 What is Karnaugh map? Simplify the given expression using Karnaugh's map and draw the logic Circuit using NAND gate only. 10
 $F(a,b,c,d)=\sum m(5,6,7,8,9)+d(10,11,12,13,14,15)$.