

DEPARTMENT OF ELECTRONICS AND TELECOMMUNICATION ENGINEERING

LAB MANUAL

Year & Semester: 2nd Year, 4th Semester

Subject Code/Name: PR-3, Digital Electronics Lab

Digital Electronics

Lab

| (e)· | LABORATORY WORK INSTRUCTI | ON | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
|----------------------|---------------------------|-------------|--|
| Date of Preparation: | Prepared by: | Jas. | Counter Signature of the HOD : |
| 20-12-2010 | Verified by: | | AA) |
| Semester:4th | Branch : Electrical. | Name of the | e Practical with Code : Digital Electronics Lab(PR- |
| | | | |

Name of the Experiment: Familiarization of digital trainer kit-AET-21

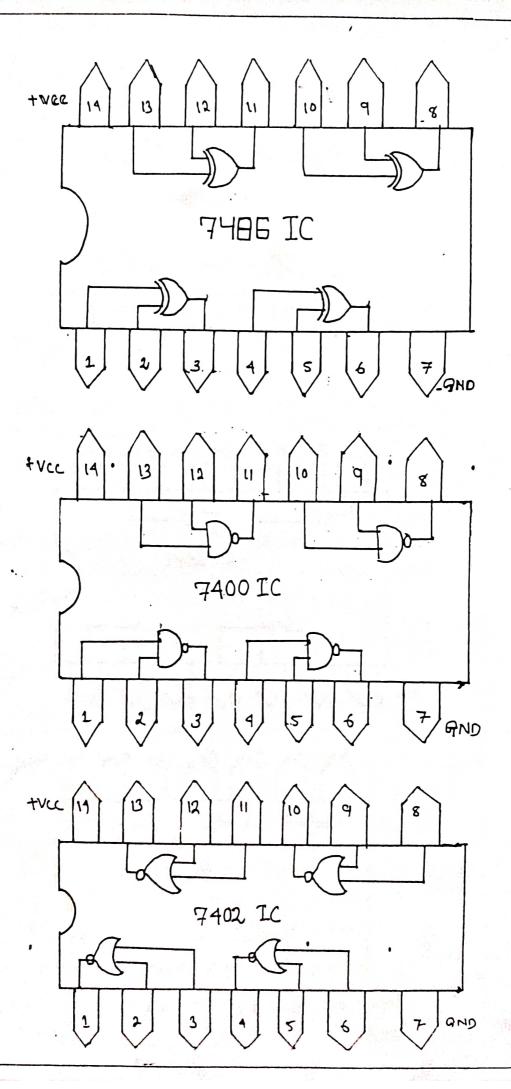
EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

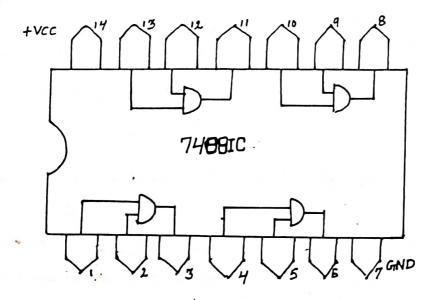
- Basic Logic Trainer Kit-AET-21
- IC-7400, IC-7402, IC-7404, IC-7408, IC-7432, IC-7486.

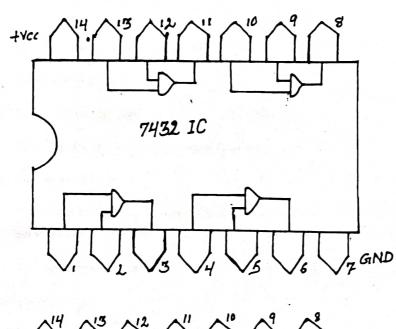
PROCEDURE:

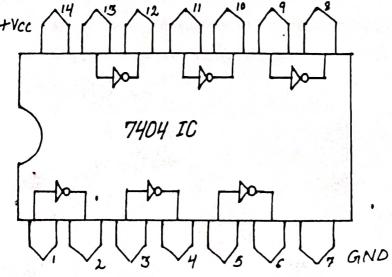
- Take the IC 7400.
- Study the no of pins present in it.
- Study the +VCC & GND pins.
- Point out the other pins following the internal circuit diagram of the above ICs.
- Follow the above procedure for the above ICs.

- Do not connect the IC to any other power supply.
- · Handle it carefully.









| | LABORATORY WORK INSTRUCTION | and and the second seco | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
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| Date of Preparation: | Prepared by: July Da | | Counter Signature of the HOD : |
| 20-12-2010 | Verified by : | | A |
| Semester 4+h | Branch : Electrical. | Name of the Practical v | with Code: 'Digital Electronics Lab(PR-2) |
| Name of the Experim | ent: Verify the truth tables of AND, OR, I | NOT NOR NAND XOR XN | OR Gates |

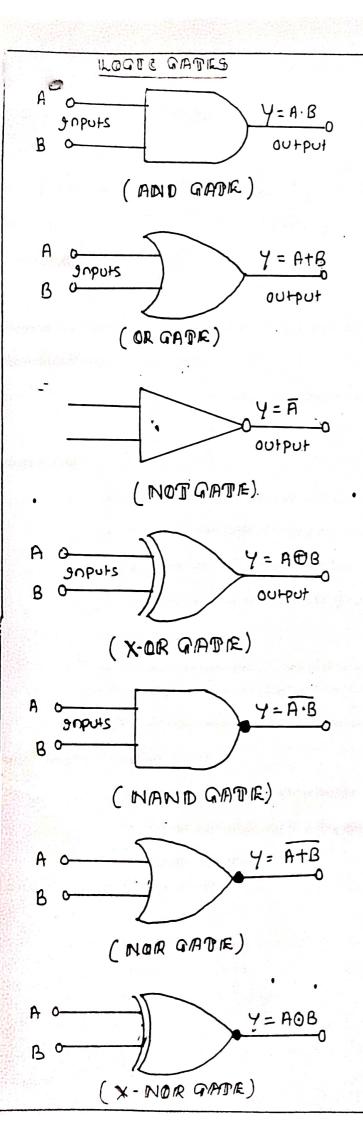
EQUIPMENT/TOOLS/ACCESSORIES REQUIRED :

- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

PROCEDURE:

- Take a basic logic trainer kit (AET-21)
- Draw the truth table.
- Draw the logical diagram by solving the truth table.
- · Connect the kit according to logic diagram.
- · Switch on the kit.
- Verify the truth table by giving logical zero or one from logic input switches connected to the input of the gates and output is found at logic indicators connected to the output.
- If indicator glows then it represents logic 1 and if not then it is taken as logic 0.

- After connections of all connectors then only switch on the power supply.
- Do not disconnect the IC during operation.
- · Handle it carefully.



TRINTH TABILE

| INP | OUTPUT | |
|-----|--------|----------|
| 14 | В | Y= A . B |
| 0 | 0 | ·- 0 |
| 0 | | Ο. |
| | 0 | 0 |
| 1 ' | | 1 |

| 1NP | OUT PUT! | |
|-----|----------|---------|
| A - | B. | OUTPUT! |
| 0 | • 0 | 0 |
| 0 | 1 | 1 |
| | 0 | 1 |
| | | 1 |

| 30001 | output |
|-------|--------|
| A | 8=Ā- |
| 0 | 1 |
| 1 | 0 |

| | | _ |
|--------------|---------|---|
| INP | OUTPUT. | |
| A | Y=ABB | |
| 0 | 0 | 0 |
| 0 | 1 | |
| 1 | 0 | 1 |
| gi a share n | 5 - 1 | 0 |

| IMP | IMPUTS | | | | |
|-----|--------|------------------|--|--|--|
| A | B. | OUTPUT Y= A·B | | | |
| ٥ | 0 | 01 | | | |
| O | 8 2 | 1 | | | |
| 1 | 0 | l | | | |
| 1 | 1 | Q | | | |

| りつ | INPUTS | | |
|----|--------|-----------------|--|
| A | B | OUTPUT Y=ATB | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| | 0 | 0 | |
| | | 1 0 | |

| TNPUTS | | OUTPUT |
|----------------|-----------|---------|
| A | B | Y = 40B |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| | 0 | 0 |
| AN YEAR STREET | NOTE HELD | 1 1 2 |

| (6) | LABORATORY WORK INSTRUCTION | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
|----------------------|-----------------------------|--|
| Date of Preparation: | Prepared by: July 2as. | Counter Signature of the HOD : |
| 20-12-2010 | Verified by: | |
| Semester:4# | Branch : Electrical Nar | ne of the Practical with Code : Digital Electronics Lab(PR-2 |
| Nove of Al S | | |

Name of the Experiment: Implement various Gates by using universal properties of NAND and NOR Gates, Verify the truth tables.

EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

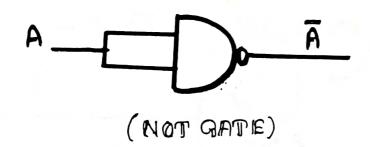
- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

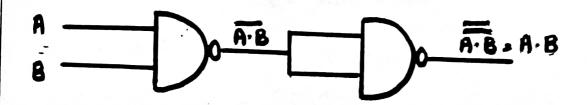
PROCEDURE:

- Take a basic logic trainer kit (AET-21)
- Draw the truth table of individual basic gates.
- Draw the logical diagram of each basic gates by implementing the property of Universal Gates.
- Connect the kit according to logic diagram.
- Switch on the kit.
- Verify the truth table of each gate by giving logical zero or one from logic input switches connected to the input of the gates and output is found at logic indicators connected to the output.
- If indicator glows then it represents logic 1 and if not then it is taken as logic 0.

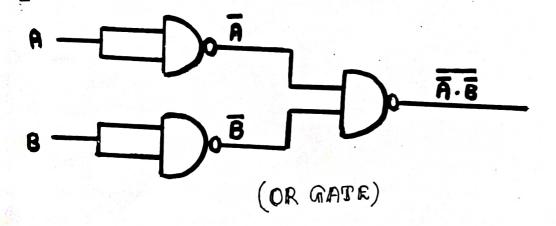
- After connections of all connectors then only switch on the power supply.
- Do not disconnect the IC during operation.
- Handle it carefully.

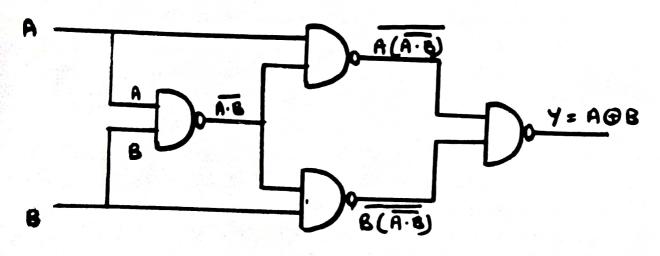
REALIZATION OF LOGIC GATES BY WSING WAND GATIE



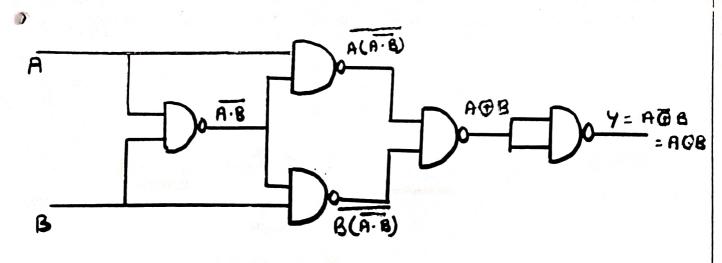


(AND GATE).



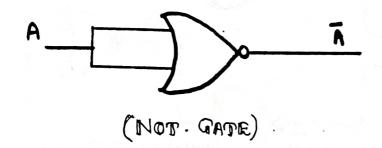


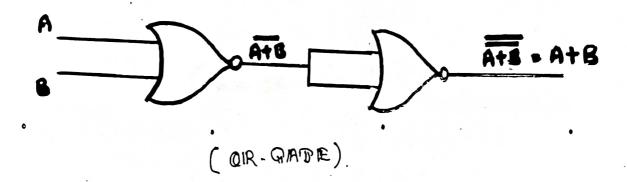
(EX- OR GATE)

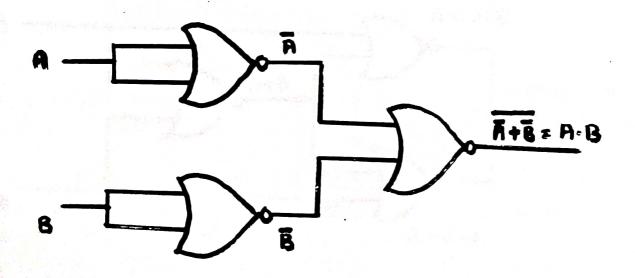


(EX - NOR GATE)

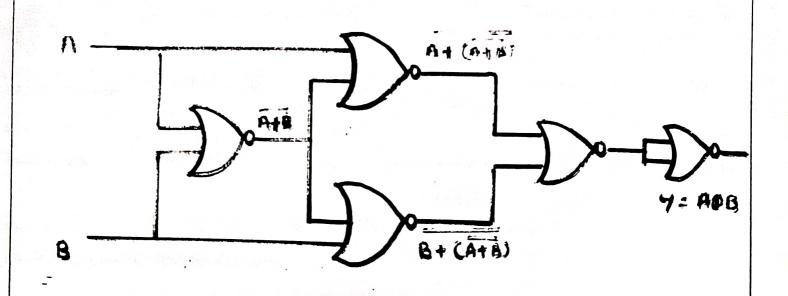
PRAIMEATION OF LOGIC GATES BY USING NOR WATES





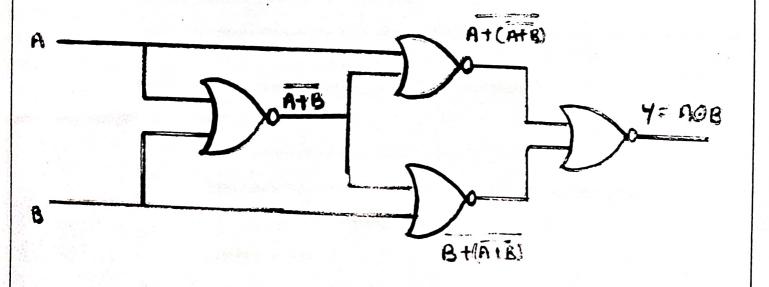


(AND GATE)



(IEX- OR GATE)

0



(EX- NOR GATE)

| (6) | LABORATORY WORK INSTRUCTION | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
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| Date of Preparation: | Prepared by: July Das. | Counter Signature of the HOD : |
| 20-12-2010 | Verified by: | |
| Semester:4-1h | Branch : Electrical | Name of the Practical with Code : Digital Electronics Lab(PR-2) |
| | | |

Name of the Experiment: Verify the truth table of Half adder & Full adder using logic circuits.

EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

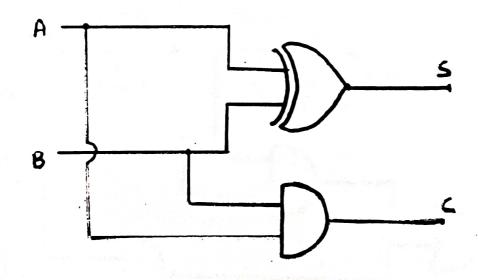
PROCEDURE:

- Draw the truth table for difference and borrow.
- From the truth table design the logic diagram for the above.
- According to the logic diagram connect the logic trainer kit (AET-21)
- Before giving the supply check the circuit again.
- Operate the input switch in different states i.e. (00,01,10,11) and check the output by the help of indicator
 LED.
- Confirm about the output by checking the result with truth table.

- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.

CKT DIAGRAM FOIR WAILF ADDIER:

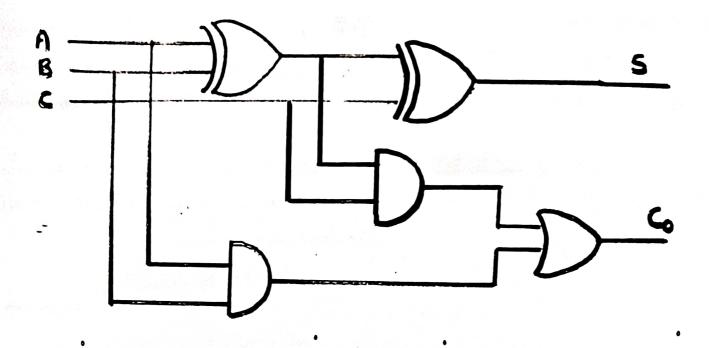
0



TRUTH TABLE FOR HALL ADDER :-

| INPUT | | OUTPUT | |
|-------|---|--------|-----|
| A | B | S | C . |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | L | 0 |
| 1 | 1 | 0 | 1 |

COR DUAGRAM FOR FILLILL ADDER.



PIRMOH DABING FOR FULL ADDER:

| gaputs | 00H | PU+ | |
|--------|-----------------------|---|-------------------------------------|
| В | . с | .S | С |
| 0 | O | 0 | 0 |
| 0 | 1 | 1 | O |
| | 0 | 7 | O |
| | | 0 | 1 |
| 0 | D | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 7 | 0 | 1 |
| 1 | (| 1 | 1 |
| | B 0 0 1 1 | B C O O O O O O O O O O O O O O O O O O | B C S O O O O I 1 I O I I O O O O O |

| | | TELECOMMUNICATION ENGG. |
|----------------------|----------------------------|---|
| Date of Preparation. | Prepared by: Verified by: | Counter Signature of the HOD: |
| Semester 44h | Branch : Electrical | Name of the Practical with Code : Digital Electronics Lab(PR-2) |

EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

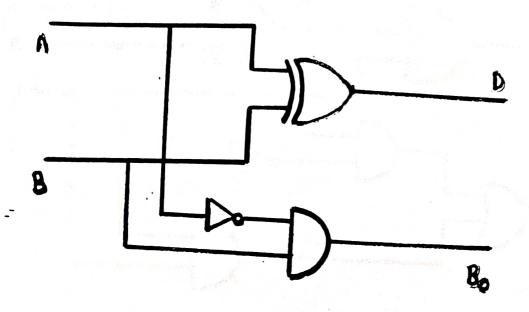
- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

PROCEDURE:

- Draw the truth table for difference and borrow.
- From the truth table design the logic diagram for the above.
- According to the logic diagram connect the logic trainer kit (AET-21)
- Before giving the supply check the circuit again.
- Operate the input switch in different states i.e. (00,01,10,11) and check the output by the help of indicator LED .
- Confirm about the output by check the result with truth table.

- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.

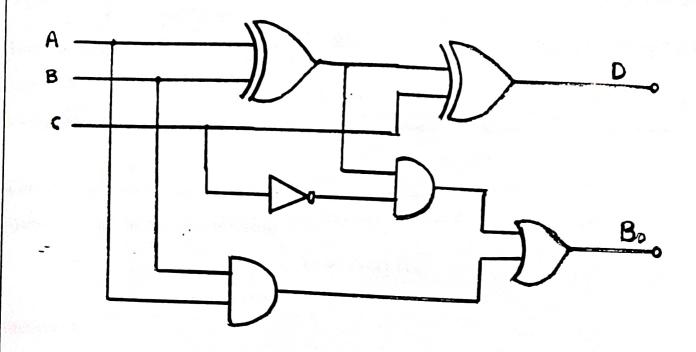
I'M DIAGRAM FOR HALF SUBTRACTOR:



TRUMPASTERBULLEOR HALLE SWEDPRACTOR:

| gnp | UHS | OUTPUTS | | |
|-----|-----|---------|--------|--|
| A | B | B | i Bo 1 | |
| 0 | 0 | 0 | - O - | |
| 0 | _ 1 | 1 | 1 | |
| 1 | 0 | | . 0 | |
| 1 | 1 | 0 | 0 | |

JING DIAGRAM FOR FUILL SUBTRACTER:-



TRUTH TABLE FOR FULL SUBSTRACTOR:

| Service Control of the Control of th | gapors | Outp | 10+ | |
|--|--------|------|-----|---|
| A | B | | B | n |
| 0 | 0 | 0 | 0 | 0 |
| 0 | | 1 | 1 | 1 |
| 0 | L | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | | ð |
| L | 0 | 1 | 0 | 0 |
| | | ٥ | 0 | 0 |
| • • | | | 1 | 1 |

| (a) | LABORATORY WORK INSTRUCTION | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
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| Date of Preparation: | Prepared by: July &cus | Counter Signature of the HOD: |
| Semester: 41h | Branch : Electrical | Name of the Practical with Code : Digital Electronics Lab(PR-2) |
| Name of the Experime | ent: Implement a 4-Bit binary to gray code | |

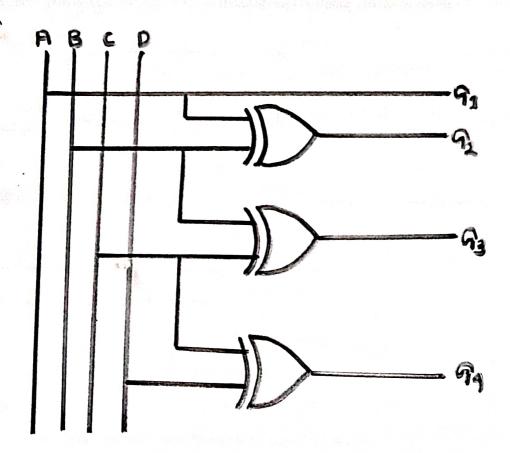
EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

PROCEDURE:

- Draw the truth table for binary to gray code conversion.
- From the truth table design the logic diagram for the above.
- According to the logic diagram connect the logic trainer kit (AET-21)
- Before giving the supply check the circuit again.
- Operate the input switch in different states i.e. (0000 to 1111) and check the output by the help of indicator LED.
- Confirm about the output by check the result with truth table.

- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.



(CKT DIAGRIAM FOR BINIARY TO GRAY CODE CONVERSION)

TRIUTH PAIBLE:--

| - | | | | | | | |
|-----------------|----------|-------|----|------|----|----------------|----|
| | 95 | ztuge | | | | PUTS | |
| _B ₁ | B2 | ₽3 | B4 | S4 . | જ્ | ज ₃ | 59 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | O | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | L | 0 | 0, | 0 | 1 | 1 | 0 |
| 0 | 1 | 6 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 10 | <u>a</u> | 1 | 1 | 0 | L | 0 | 0. |
| 1 | 0 | 0 | .0 | 1 | 1 | 0 | |
| F | 0 | 0 | 1 | 1 | 1 | | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | | 1 |
| 1 | 1 | 0 | 0 | 1 | | 4 | 0 |
| 1 | - | | 1 | 1 | 0 | 1 | 0 |
| + | | 0 | | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | O | 0 | 1 |
| 1 | J | 1 | 1 | 1 | 0 | 0 | 0 |

| (0) | LABORATORY WORK INSTRUCT | ION | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
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| Date of Preparation: | Prepared by: July | Jus. | Counter Signature of the HOD : |
| 20-12-2010 | Verified by : | _ | |
| Semester: 4th | Branch : Electrical | Name of the Pract | Lical with Code: `Digital Electronics Lab(PR-2) |
| Name of the Francis | anti lambana da da la la da | | 40.00 |

Name of the Experiment: Implement a single bit digital comparator.

EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

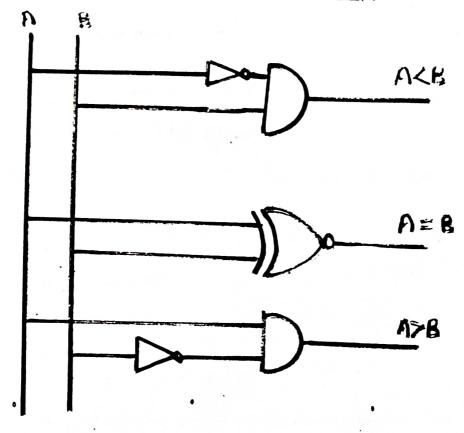
- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

PROCEDURE:

- Draw the truth Table for single bit digital comparator.
- From the truth table design the logic diagram.
- According to the logic diagram connect the logic trainer kit (AET-21)
- Before giving the supply check the circuit again.
- Operate the input switch in different states i.e. (00,01,10,11) and check the output by the help of indicator LED .
- Confirm about the output by checking the result with truth table.

- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.

CUT DUAGRAM FOR SINGLE BET COMIPIAIRATION :--



TIRWITH TABLE FOR SINGLE BIT COMPARATOR:

| 90 | purs | OUTPUTS | | |
|----|------|---------|-----|-----|
| A | B | ALB | A=B | AZB |
| 0 | 0 | ð | 4 | O |
| 0 | 1 | 1 | 0 | 0 |
| 1_ | .0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

| (6) | LABORATORY WORK INSTRUCTION | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
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| Date of Preparation: | Prepared by: Verified by: | , Counter Signature of the HOD : |
| 20-12-2010 | Om L | CO. |
| Semester: 4th | Branch : Electrical | Name of the Practical with Code : Digital Electronics Lab(PR-2) |
| Name of the Francisco | ent: Study multiplexer and demultiplexer. | |

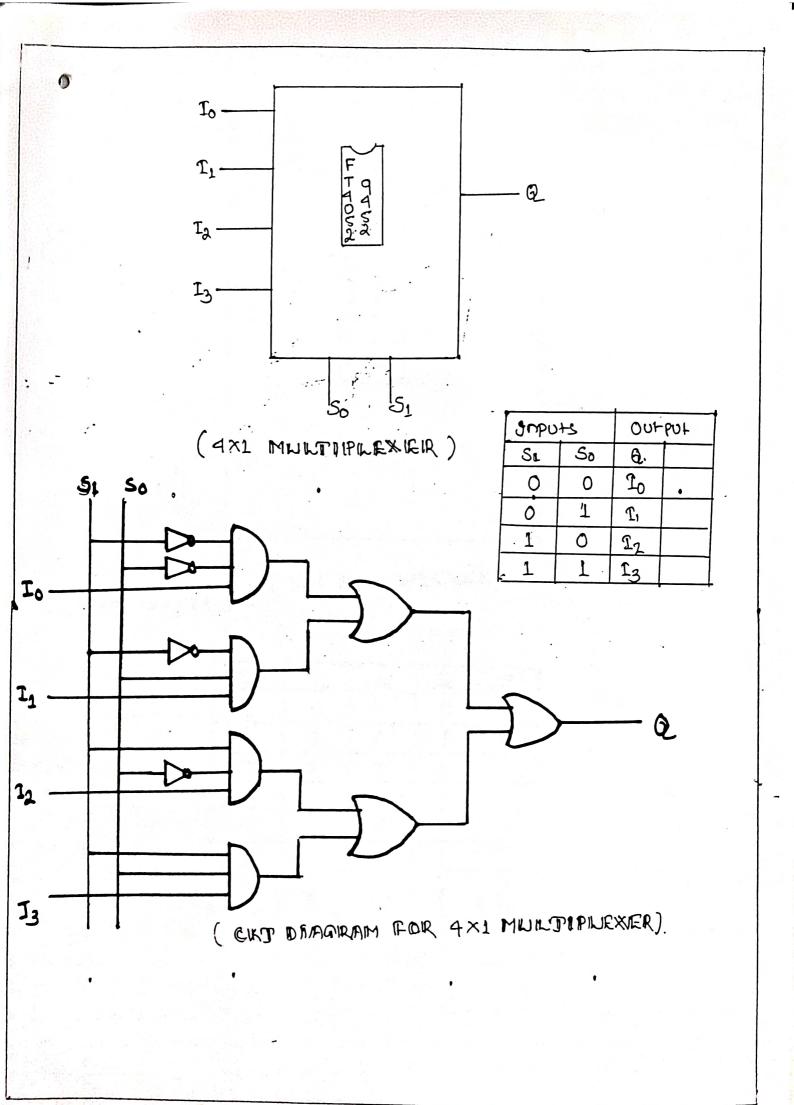
EQUIPMENT/TOOLS/ACCESSORIES REQUIRED :

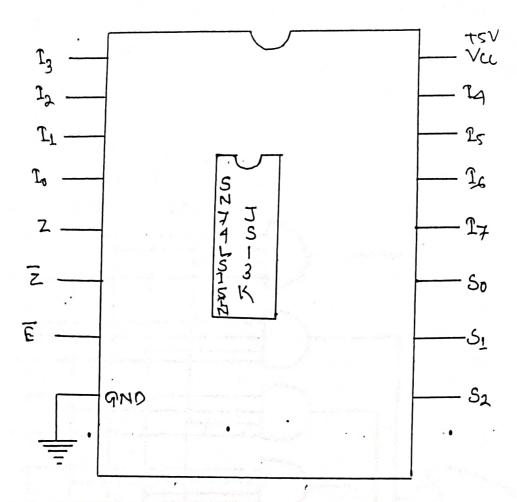
- Multiplexer Trainer Kit (AET-31)
- Connecting Wires.

PROCEDURE:

- Draw the truth Table for multiplexer and demultiplexer separately.
- From the truth table design the logic diagram.
- According to the logic diagram connect the logic trainer kit.
- Before giving the supply check the circuit again.
- Give the input for the selection line and data input line from logic indicator switches.
- Connect the output of mux and demux to output indicators.
- Switch on power supply.
- Confirm about the output by checking the result with truth table.

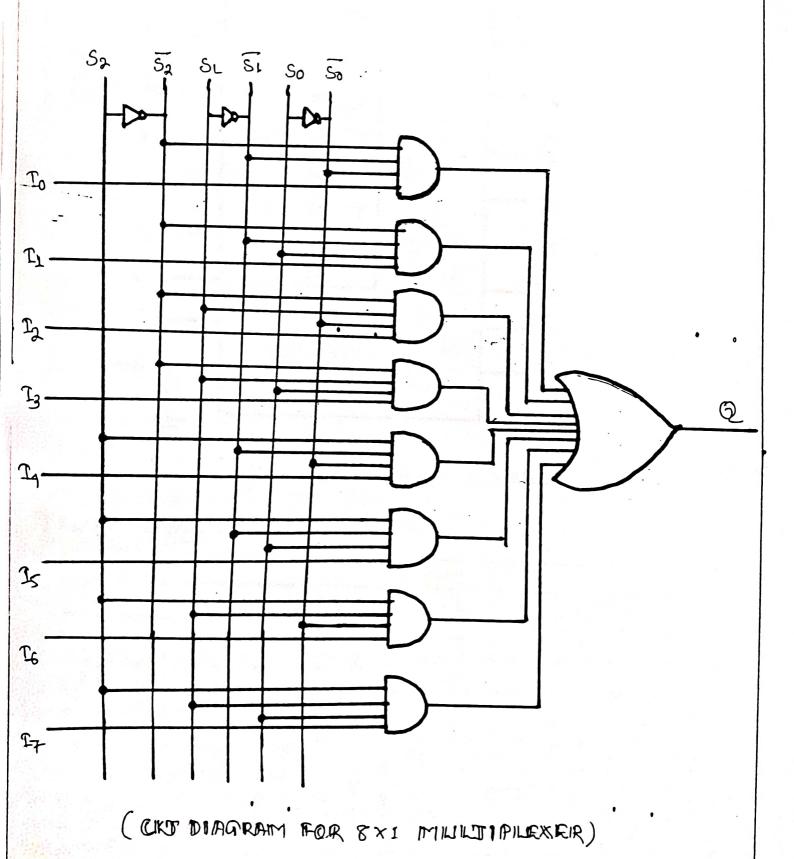
- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.

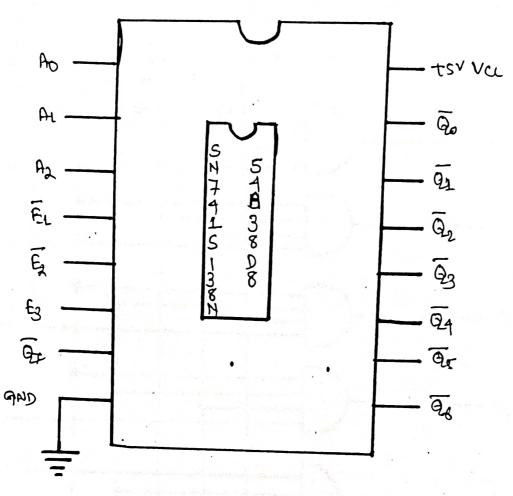




TRUTH PABILE:-- (8X1 MILLTIPILEXER)

| Person | E | Sa | SL | . So : | Q |
|--------|---|-----|-----|--------|------------------|
| | 1 | 0 | 0 | 0 | 20 |
| | L | ð | 0 | 1 | I, |
| | 1 | 0 | 1 | 0 | \mathfrak{T}_2 |
| | 1 | . 0 | 1 | 1 | 13 |
| | L | 1 | 0 | 0 | Iq |
| | 1 | 1 | 0 | 1 | L |
| 20 | 1 | L | L L | 0 | 16 |
| | 1 | -1- | 1 | 1 | Î7 |





(1 X8 DEMLUTTPILEXIER).

TRUTH TABLE :-

| Э | npoks | | | 91 0 | OUF | PUTS | • | | | |
|--------------|-------|----|--------------------------|------|-----|-----------------------|----|-----|----------------|-----|
| 52 | 51 | So | Qo | a | 02 | Q ₃ | QA | a. | a _B | Q7 |
| 0 | 0 | 0 | The second of the second | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0. | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 5-7-1 | 0 | 0 | 0 | | 0 | ٥ | 0 % | - | O |
| 0 | L | L | 0 | 0 | 0 | L | O' | 0 | 0 | 0 |
| 1 | 0 | ð | 0 | 0 | 0 | 0 | 1 | 0 | δ | 0 |
| <u> L </u> | 0 | 1_ | Q | 0 | ð | 0 | 0 | 4 | ,0 | 0 |
| 1 | 1 | 0 | 0 | 0 | ٥ | 0 | 0 | 0 | 1 | ٥ |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | O | D | 0 | . 1 |

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· · (CKT DIRAIRAM FOIR LX8 DIEM NINT I PLEXIER)

| (6) | LABORATORY WORK INSTRUCTION | | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
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| The state of the s | Prepared by : | C. | |
| Date of Preparation: | Trepared by . | Lyz & as , | Counter Signature of the HOD: |
| 20-12-2010 | Verified by : | 2 | |
| Semester 4.4 | Branch : Electrical. | Name of the Practical | with Code : Digital Electronics Lab(PR-2) |
| Name of the Experime | ent: Study of Flip-Flop (S — R f | lip flop) | |

EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

- Basic Logic Trainer Kit-AET-21
- Connecting Wires.

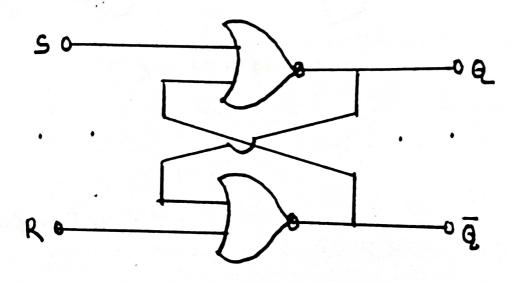
PROCEDURE:

- Draw the truth Table for S-R flip-flop.
- From the truth table design the S-R flip flop circuit using NAND & NOR Gate separately.
- According to the logic diagram connect the logic trainer kit (AET-21)
- Operate the input switch in different states i.e. (00,01,10,11) and check the output by the help of indicator LED.
- Confirm about the output by checking the result with truth table.

- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.



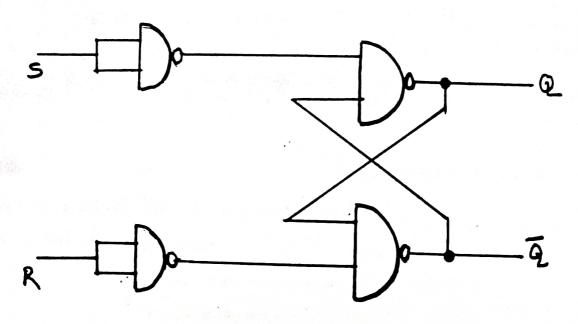
(BLUCK DIAGRAM OF S-R FLIP-FLOP).



(CIKT DIAGRAM OF 5-R IFILIP FLOOP WING WOR).

| Supurs | | outputs | | |
|--------|---|----------|----|--|
| S | R | Q | ତ୍ | |
| _ D | 0 | HOUD | | |
| 0 | L | 0 | L | |
| 1 | 0 | L | 0 | |
| 1 | L | INVA UD. | | |

(FRUTH TABILE OF S-R FLIP FLOP).



(3-R FLEP FLOP HAIND).

TRUTH TABLE :--

| 3 NPUHS | | | outputs | | |
|---------|-----|---|---------|------|----------|
| S | R | Ē | la | Q_ | © |
| 0 | O | 1 | 1 | 02 | Q |
| O | 1 | 1 | 0 | 0 | L |
| 1 | م ر | 0 | 1 | T | Õ |
| 1. | | D | 1 | PNVA | 4D |

| | LABORATORY WORK INSTRUCTION | DEPARTMENT: ELECTRONICS AND TELECOMMUNICATION ENGG. |
|----------------------|------------------------------|---|
| Date of Preparation: | Prepared by : Verified by : | Counter Signature of the HOD: |
| Semester 4th | Branch : Electrical. | Name of the Practical with Code : Digital Electronics Lab(PR- |

Name of the Experiment: Study of Flip-Flops (J-K flip-flop,D flip-flop,T flip-flop)

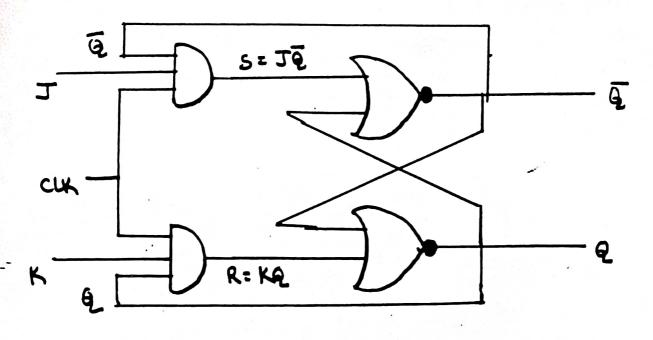
EQUIPMENT/TOOLS/ACCESSORIES REQUIRED:

- Basic Logic Trainer Kit-N-24
- Connecting Wires.

PROCEDURE:

- Draw the truth Table for J-K flip-flop,D flip-flop,T flip-flop.
- From the truth table design the logic diagrams.
- According to the logic diagram connect the trainer kit.
- Before giving the supply check the circuit again.
- Connect the inputs from push button switches A & B and clock input from the clock switch.
- Switch on the power supply.
- Give input 0 or 1 from logic switches by push on or off switches A or B.
- Confirm about the output by checking the result with truth table.

- Do not connect the IC to any power supply directly.
- After connections of all connectors then only switch on the power supply.
- Don't disconnect the IC during operation.
- Handle it carefully.



(CIKT DIAGRIM FOR J-K THUP-FLOP)

JRNPH PAIBLE:

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| previous | JUDOL | | Neut |
|----------|-------|---|------|
| ලා | J | K | anti |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | L | 0 | 1 2 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | L |
| L | 0 | 1 | 0 |
| L | L | 0 | 1 |
| L | 1 | 1 | 0 |